New Circuit Topology for Fault Tolerant H-Bridge DC-DC Converter

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***Abstract*— The paper describes a new design for a fault tolerant H-bridge DC-DC converter. Fault tolerance is achieved using a multilevel converter topology in combination with a PWM control strategy allowing a large set of converter switching states to produce bi-directional power flows at any required output voltage. For a given converter open-circuit or short-circuit fault, all potential switch combinations are compared in terms of converter losses and output voltage harmonics to identify the most suitable switching combinations to achieve the pre-fault output voltage level. The fault tolerant ability of the proposed converter to recover the required output voltage is verified by both computer simulations and experimentally using a 1 kW laboratory set.**

***Index Terms*— DC-DC power conversion, Fault tolerance, Harmonic analysis, Multilevel system, Losses.**

I. Introduction

DC-DC converters are commonly used in a wide variety of applications, including a number of critical applications in which very high levels of reliability are required because the loss of converter operation can have serious consequences. For example, control of a car is lost when the supply voltage for a brake-by-wire system has collapsed due to a converter failure. Another critical application is the use of a DC-DC converter in low-power refrigeration applications developed for use in an ambulance to maintain saline temperature within a specific range for immediate injection into a patient [1]. In such an application, the loss of control of the converter voltage can lead to a temperature difference of several degrees and serious medical complications.

In order to achieve highly reliable DC-DC conversion systems, N+M redundancy concepts have been proposed in the past [2], [3]. This is a costly option in which one or more additional DC-DC converters are connected in parallel to achieve the required levels of redundancy in case of failure of the main converter. More recently, it has been shown that multilevel DC-AC converter topologies can be operated as fault tolerant circuits [4]-[6]. Multilevel DC-DC converters with multiple dc sources and no magnetic storage components have been proposed recently to achieve variable dc output voltage operation [7]. Initial investigations of the multilevel concept as applied to DC-DC converters for fault tolerant applications have also been presented [8]-[10]. Khan et al, for example, described a pseudo fault tolerant modular multilevel DC-DC converter [9] which could continue to operate in the event of a short circuit fault in any of the series connected modules; the circuit, however, could not operate successfully if one of its power devices had experienced an open circuit fault, as recognized by the authors.

In this paper, a "true" fault tolerant multilevel DC-DC converter based on the multilevel H-bridge inverter topology proposed by Ceglia et al [11] is developed and its fault tolerant behavior is investigated. The original circuit, as proposed by Ceglia et al, suffers from a number of potential problems and drawbacks when operated as a DC-DC converter including high operational losses and long term reliability problems, as some of the switches are required to conduct permanently. In this study, a new PWM control strategy is developed and applied to a modified circuit topology, in which the original converter is extended by the addition of an extra switching leg and bi-directional selector switches, to overcome these problems.

Fig.1 shows the proposed H-bridge with Auxiliary Leg and Selector Cells (HBALSC) fault tolerant multilevel DC-DC converter. The main H-bridge power circuit (power devices S1-S4 and diodes D1-D4) is extended by two auxiliary switches (SA1/DA1 and SA2/DA2), three selector cells (power devices S5-S7, diodes D5-D16 and bidirectional switches SE_1-SE_3) and six additional bi-directional switches (SE_4-SE_9) to form the multilevel topology. Fault tolerant operation is achieved by using different switching states and controlling the PWM duty cycles of the individual switches to produce the required average output voltage with the minimum number of switches and power diodes.

The paper examines different fault scenarios to demonstrate the full fault tolerant capacity of the proposed converter. Different combinations of switching states and duty cycles are evaluated and compared in terms of power losses and generated output voltage harmonics to identify the most suitable conduction states to achieve the required output. The variety of switching combinations and PWM duty cycles

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provide fault tolerant operation.

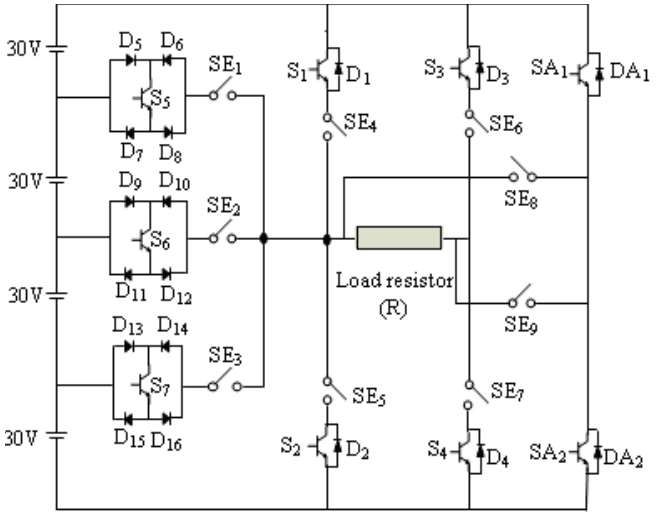

Fig. 1. Power circuit of the HBALSC multilevel DC-DC converter

II. Operating Principles of the Proposed Converter

The operation of the H-bridge, DC-DC HBALSC converter (connected to a resistive load) under normal operating conditions is described in this section.

The HBALSC converter allows bi-directional power flow and, depending on the switching states used, can produce nine different output voltage levels (-120V, -90V, -60V, -30V, 0V, 30V, 60V, 90V, 120V) when operating without PWM control, as shown in Table I. The application of PWM control allows operation at any required average voltage between -120 V and +120 V. It should be noted here, that the circuit cannot achieve the redundancy needed for fault tolerant operation by varying the switching states alone; each voltage level can be generated by only one switch combination as shown in Table I. The current path for the conduction state corresponding to an output voltage of 30V is shown in Fig. 2 as an example.

TABLE I
SWITCHING STATES FOR EACH VOLTAGE LEVEL

Voltage levels	Current paths
30V	D13, S7, D16, SE3, SE7, S4
60V	D9, S6, D12, SE2, SE7, S4
90V	D5, S5, D8, SE1, SE7, S4
120V	S1, SE4, SE7, S4
0V	SE5, S2, SE7, S4
-30V	S3, SE6, SE1, D6, S5, D7
-60V	S3, SE6, SE2, D10, S6, D11
-90V	S3, SE6, SE3, D14, S7, D15
-120V	S3, SE6, SE5, S2

In the following analysis, only forward power flow switch combinations will be considered (i.e. no negative voltage switching states will be described).

Fig. 3 shows four output voltage levels V_{Ln} with PWM control at a fixed duty cycle D and a constant switching frequency. Assuming each voltage level is applied for an equal time T/4 (Fig.3), the average output voltage V_0 can be calculated from:

$$Vo = \frac{D}{m}.\sum_{n=1}^{m} V_{Ln} \quad (1)$$

where D is the duty cycle, m is the number of voltage levels and V_{Ln} is the output voltage associated with level n.

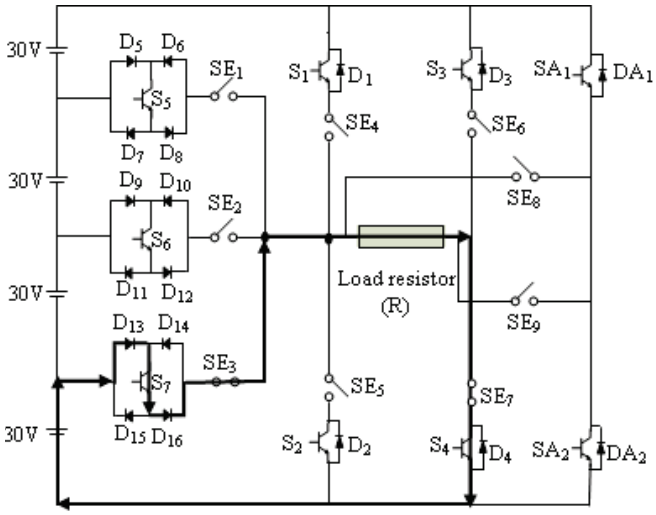

Fig. 2. Current path for conduction state corresponding to 30V output voltage

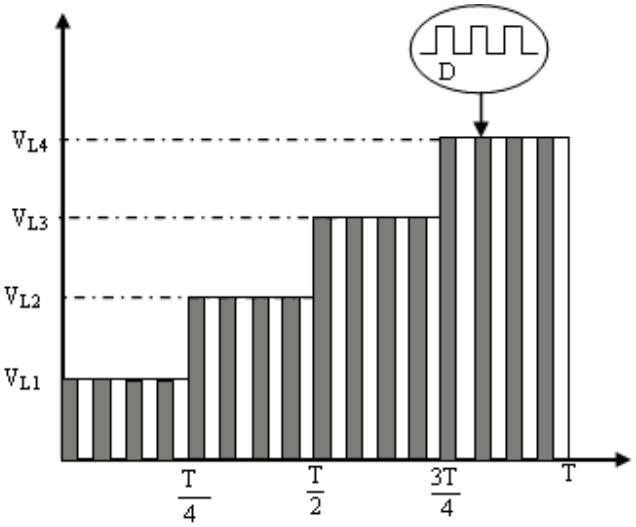

Fig. 3. Output voltage levels

Equation (1) shows that the different switching states can produce a large number of possible output voltages when combined with all the possible values of converter duty cycle D. For example, Table II shows five possible switching states combinations with different values of D to generate a 60V average output voltage.

The operation of the converter was investigated using PSpice simulation and verified experimentally. Models provided by semiconductor manufacturers were used for the power devices and diodes. A 1kW prototype IGBT test circuit was also constructed to test the operation of the proposed circuit topology. The converter was fed from four 30V power supplies and operated with a 5 kHz switching frequency.

TABLE II
POSSIBLE SWITCH COMBINATIONS TO GENERATE 60V AVERAGE OUTPUT

State Number	Output Voltage levels			PWM duty cycle D	Average Output Voltage
	30V	90V	120V		
1	yes	yes	yes	0.75	60 V
2	yes	-	yes	0.80	60 V
3	-	yes	yes	0.57	60 V
4	-	yes	-	0.67	60 V
5	-	-	yes	0.50	60 V

Figs. 4-6 show measured output voltages for three different device switching combinations (states 1,3 and 5 in Table II). It is apparent from the figures that PWM control allows alternative switching options for the required output voltage level. Converter operation with the same switch combinations was also simulated using PSpice showing good agreement with measurement.

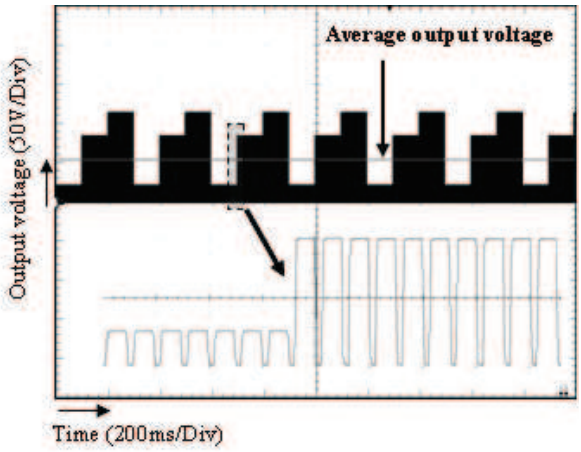

Fig. 4. Measured output voltage waveform for V_o = 60V; PWM duty cycle D = 0.75 with voltage levels of 30V, 90V and 120V

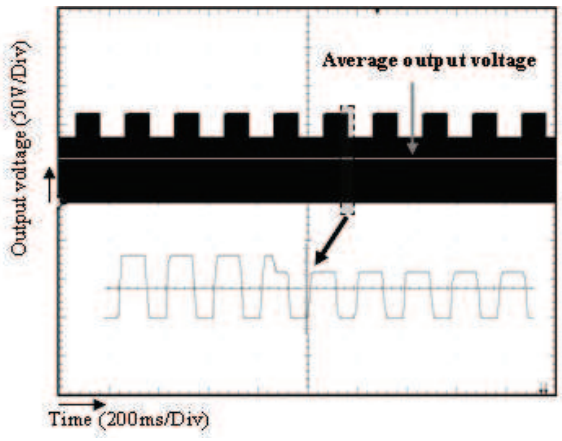

Fig. 5. Measured output voltage waveform for V_o = 60V; PWM duty cycle D = 0.57 with voltage levels of 90V and 120V

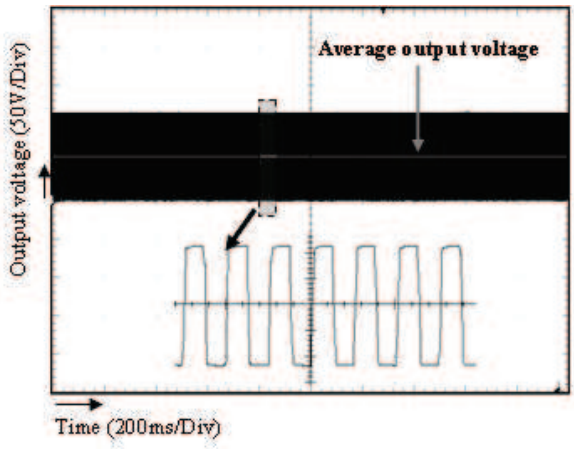

Fig. 6. Measured output voltage waveform for V_o = 60V; PWM duty cycle D = 0.5 with voltage level of 120V

III. EVALUATION OF CONVERTER LOSSES AND HARMONIC CHARACTERISTICS

In this section, different switching combinations will be evaluated in terms of the resulting converter power losses and output voltage harmonics in order to investigate the operating characteristics of the converter and identify the switch combinations needed to achieve the best overall performance for a given output voltage.

A. Converter power losses

Converter conductions and switching power losses and the resulting converter efficiencies when operating at two output voltages of 45 V and 75 V with different switch combinations were calculated and the results are shown in Tables III and IV. Output voltage levels V_{Ln} are lower than the values of the input power supply voltages because of the conduction voltage drops across the converter devices.

The lowest power losses are achieved when operating the converter with one output voltage level of 120V where the current path contains only two power devices (S_1 and S_4). In contrast, the highest losses are obtained when the converter is operated with the maximum number of output voltage levels when the current flows through more than two power devices and two diodes increasing the total power loss. It is also evident that losses are a function of the duty cycle. A larger duty cycle means longer conduction times and higher power losses.

B. Harmonic analysis of converter output voltage waveforms

Power switching devices produce harmonics because of their non-linear characteristics. In this section, the harmonic content of converter output voltage waveforms when operating at output voltages of 45 V and 75 V with different switch combinations were calculated and the results are shown in Figs.7-8.

TABLE III
CALCULATED POWER LOSSES AND EFFICIENCIES; V_O = 45 V

Output Voltage levels				V_{Ln} (V)	PWM duty cycle D	Average Output Voltage	Power Losses (W)	Efficiency (%)
30 V	60 V	90 V	120 V					
Yes	Yes	Yes	Yes	V_{L1}=27.02 V_{L2}=56.50 V_{L3}=86.03 V_{L4}= 118.3	0.60	45	31.28	84.5
Yes	Yes	Yes	-	V_{L1}=27.02 V_{L2}=56.50 V_{L3}=86.03	0.75	45	30.84	85.9
-	Yes	Yes	-	V_{L1}=56.50 V_{L2}=86.03	0.60	45	28.71	89
-	-	-	Yes	V_{L3}=118.3	0.34	45	25.53	92.8

TABLE IV
CALCULATED POWER LOSSES AND EFFICIENCIES; V_O = 75 V

Output Voltage levels				V_{Ln} (V)	PWM duty cycle D	Average Output Voltage	Power Losses	Efficiency
30 V	60 V	90 V	120 V					
Yes	Yes	Yes	Yes	V_{L1}=27.02 V_{L2}=56.50 V_{L3}=86.03 V_{L4}= 118.3	1	75	34.18	92
-	Yes	Yes	Yes	V_{L1}=56.50 V_{L2}=86.03 V_{L3}=118.3	0.83	75	34.21	92.7
-	-	Yes	Yes	V_{L1}=86.03 V_{L2}=118.3	0.71	75	33.41	93.6
-	-	-	Yes	V_{L3}=118.3	0.63	75	28.88	95

As expected, the frequency spectra of the output voltage waveforms have the same DC value at zero frequency. The amplitudes of the harmonic orders are different, however, mainly due to the different values of duty cycles used and the different shapes of the resulting time domain waveforms. Figs. 7 & 8 show that higher values of PWM duty cycle result in lower output voltage harmonics, regardless of the number of levels of the output voltage. For example, Fig. 7 shows that the three levels switching combination (30V, 60V, 90V and D = 0.75) produces lower output voltage harmonics than the four levels switching combination (30V, 60V, 90V, 120V and D = 0.6) with a significant reduction in the value of the first (5 kHz) harmonic. Similar results can be observed in Fig. 8 where the switching combination with D = 1 (voltage levels 30V, 60V, 90V and 120V) produces the lowest output voltage harmonics. To sum up, higher values of PWM duty cycles result in lower output voltage harmonics but at the cost of higher converter losses and lower operating efficiencies. The control of the converter is thus a compromise between these two conflicting requirements.

IV. FAULT TOLERANT INVESTIGATIONS

Assuming the occurrence of only one fault at a given time, constant input voltage, no loss of sensor signals and no connection faults, the fault tolerant behavior of the converter is evaluated using the 60 V operating states previously discussed in section 2 as an example. The converter must demonstrate the ability to detect a short circuit or an open circuit component fault and must change the switching states appropriately to recover the required average output voltage.

A. Description of the test circuit

Three IXYS power modules of the type (FIO 50-12BD) each consisting of a single IGBT and four diodes were used to implement selector cells S_5-S_7 and D_5-D_{16}. One IXYS power module (FII 40-06D), comprised of two IGBTs with two antiparrallel diodes, was used for each leg of the main H-bridge circuit (S_1-S_4, D_1-D_4) as well as the auxiliary leg (SA_1-SA_2, DA_1-DA_2). The current sensors used in the circuit were Hall-effect LEM current transducers (LTS 15-NP). Optocouplers (PC123XNNSZ0F) were used to sense a short circuit fault across the IGBTs and diodes as shown in Fig.9. A Dspic30F5015 controller was used to generate the required PWM control signals and to affect the appropriate change in circuit topology on detecting a fault.

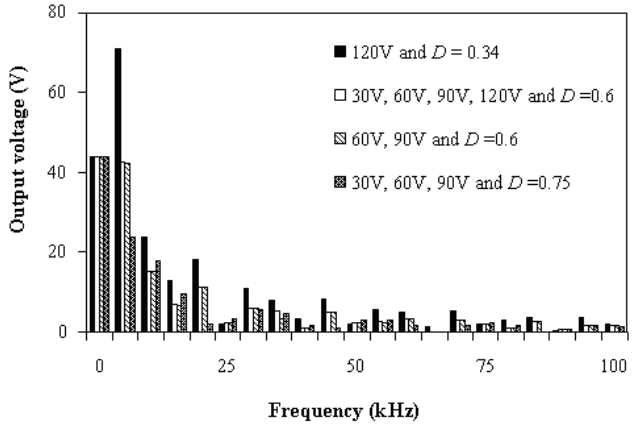

Fig.7. Harmonic spectrum of output voltage V_o = 45 resulting from switch combinations described in Table III

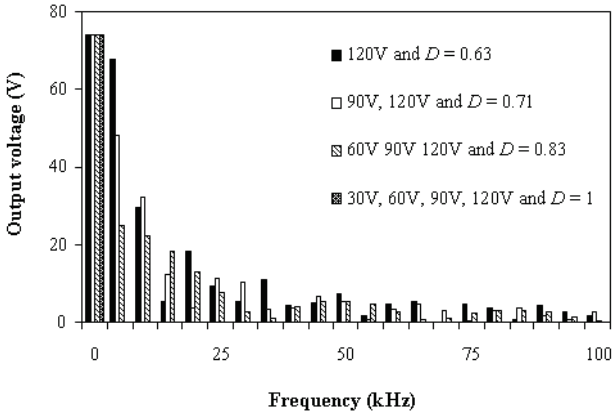

Fig.8. Harmonic spectrum of output voltage V_o = 75 resulting from switch combinations described in Table IV

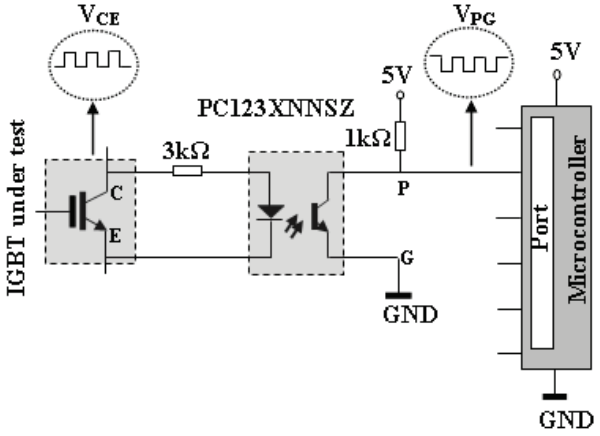

Fig.9. Voltage sensor circuit

The total number of sensors is low when compared with alternative circuit topologies [8]. However, the number of current sensors can be reduced even further by monitoring the output voltage using a Neural Network technique [12] or by using a smart IGBT gate drive with self diagnosis and fault protection [13]. The complete fault tolerant HBALSC multilevel H-bridge DC-DC converter is shown in Fig. 10.

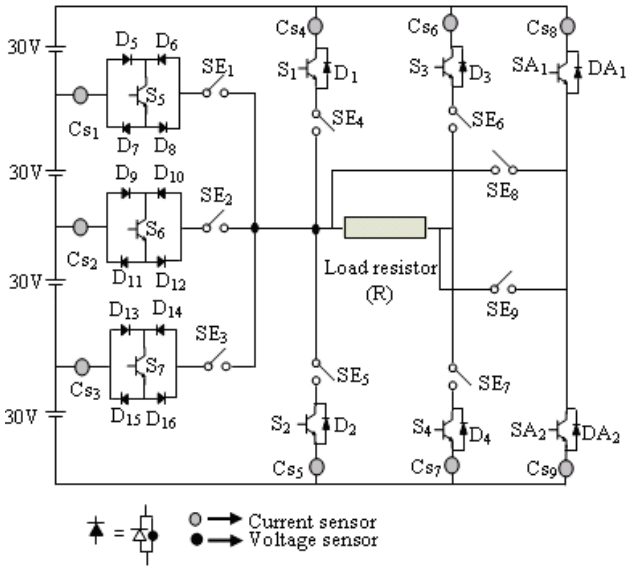

Fig.10. Fault tolerant HBALSC multilevel H-bridge DC-DC converter

B. *Open Circuit Faults*

If an open circuit fault occurs in any of the main switches S_1-S_4 or D_1-D_4, the extended additional leg must be activated. The switching sequence following an open circuit fault in S_1 is discussed here in detail as an example. A summary of controller actions following an open circuit in any device is presented in Tables V & VI in the Appendix.

Under normal operating conditions, S_1 is switched on and the controller receives a current measurement from C_{S4}. If the controller does not receive this signal while S_1 is still switched ON, the controller will flag this as an open circuit fault in S_1. The controller now identifies a new switching state that needs to be activated, in this case switches SA_1 and SE_8, in order to provide the required voltage. Fig 11 shows the timing diagram corresponding to this event. At t = 0.75ms the device becomes faulty. The current transducer delay plus the signal delay time from the controller to the drive circuit for S_1 is t_d = 50µs and the time that the controller needs to select a new switching state and to send the required gate signal is 70µs giving a total fault response time of 120µs (Fig.11). Fig.12 shows how SA_1 and SE_8 are switched on to maintain normal operation at the same output voltage when an open circuit fault occurs in S_1. After the fault, the current passing through S_1 falls to zero, but load current continues to flow through SA_1 and SE_8.

If an open circuit fault occurs in any of the selector switching cells (devices S5-S7, diodes D5-D16 and bidirectional switches SE_1-SE_3), the converter will no longer be able to produce the required average output voltage using the existing switch state combination. For example, under normal operating conditions, the converter produces output voltage levels of 30V, 60V, 90V and 120V with a duty cycle D = 0.8 to generate the required average

output voltage of 60V. If an open circuit fault were to occur in switch S_5 say, the converter is no longer able to produce a voltage level of 90V leading to the loss of the required 60V output voltage. On detecting the fault, the sequence of switching states needs to change to operate the converter at 120V and a duty cycle $D = 0.5$ (to minimize losses). Fig.13 shows measured output voltage waveform when open circuit fault occurs in S_5, showing converter operation with the above conduction states before and after the fault at the same average output voltage. The current passing through S_5 (Fig.13) becomes zero after the fault.

If an open circuit fault occurs in any of the H-bridge devices (power devices S1-S4, diodes D1-D4 and bidirectional switches SE_4-SE_7), the switches in the auxiliary converter leg (SA1 and bidirectional switch SE_8) will be activated to supply the load with same voltage.

Similar results are obtained when simulating the operation of the circuit under the same fault conditions.

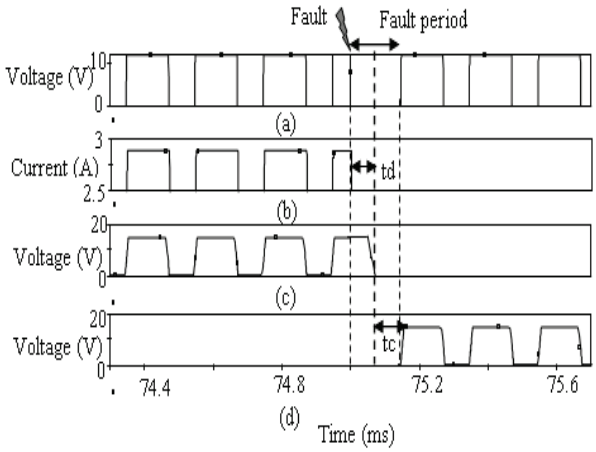

Fig.11. Timing diagram for open circuit fault in S_1 (a) output voltage (b)current sensor signal (c) gate signal of the faulty power device (d) gate signal of the on coming power device.

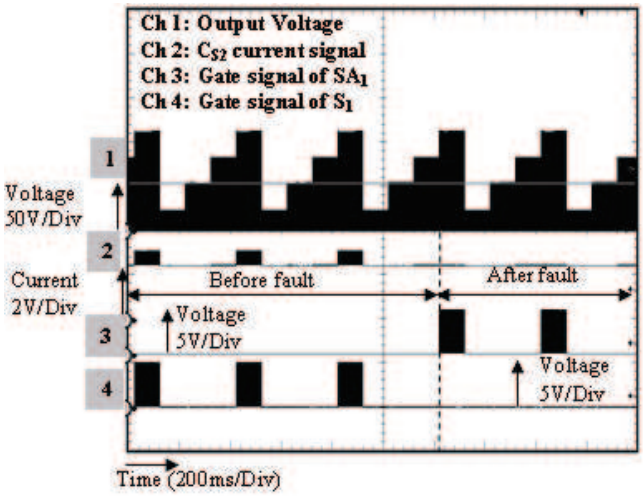

Fig. 12. Measured output voltage waveform before and after an open circuit fault in main switch S_1

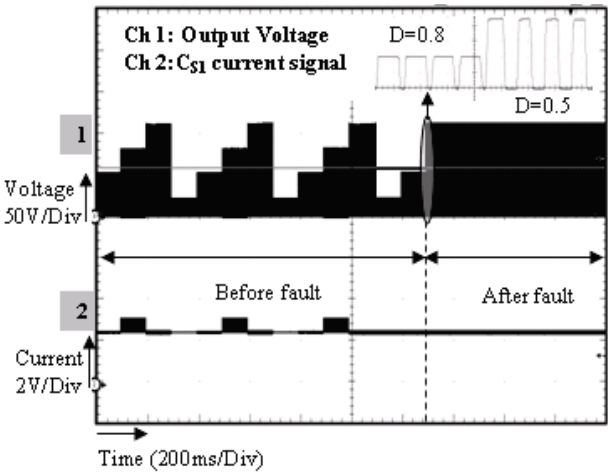

Fig. 13. Measured output voltage waveform before and after an open circuit fault in selector switch S_5

C. *Short Circuit Faults*

Diode short circuit faults are detected using the voltage sensor circuits shown in Fig. 9; short circuit faults in the power devices are detected via the gate drive circuits. On detection, short circuit faults are isolated by deactivating the corresponding selector switch. The control of the system under short circuit fault conditions is more complex when compared with open circuit faults responses due to the large number of voltage sensors and switches needed to detect and isolate each fault. The switching sequence following a short circuit fault in S_5 is discussed here as an example.

Fig. 14 shows the timing diagram corresponding to a short circuit fault in S_5. On detecting the fault, SE_1 and SE_4 are switched off and SE_8 and SA_1 switched on to initiate the new conduction state. Fig. 14 shows the timing of the events corresponding to this short circuit fault including voltage sensor delay t_S (130 μs) and controller delay t_C (70 μs). The delay when changing from one switch combination to another due to the slow response of the Omron G8P-1A4P electromechanical single-pole relays used to implement the bi-directional selector switches (SE_1-SE_9) in this experimental setup ($t_{d1} + t_{d2} = 5$ ms) is also shown.

Similar responses are required for short circuit faults in any of the main H-bridge switches. A summary of controller actions following a short circuit in any device is presented in Tables V and VI in the Appendix.

In the experimental investigation, a short circuit fault condition was generated by switching an additional power device connected in parallel with the device to be tested. Fig.15 shows the measured output voltage waveform before and after a short circuit fault selector switch S_5.

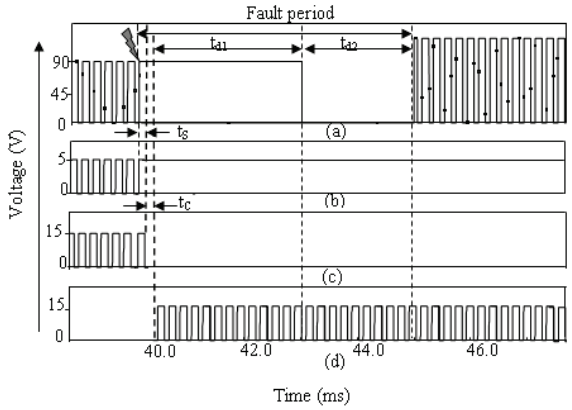

Fig.14: Timing diagram for short circuit fault in S_5 (a) output voltage (b) voltage sensor signal (c) gate signal for the faulty power device (d) gate signal of the on coming power device.

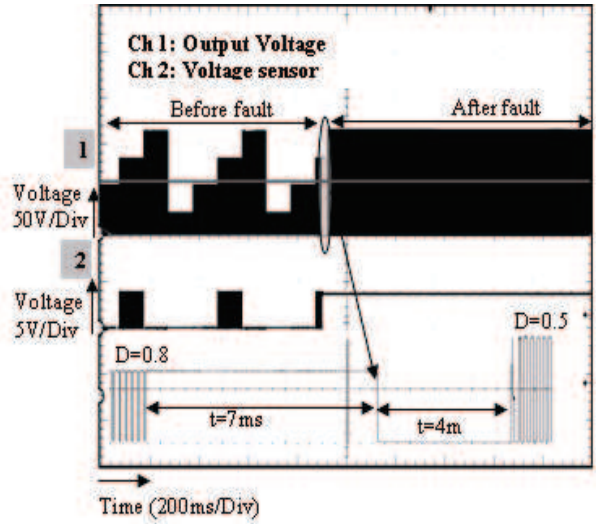

Fig. 15. Measured output voltage waveform before and after a short circuit fault in selector switch S_5

V. Conclusion

A novel, fault tolerant multilevel H-bridge DC-DC converter topology has been presented in this paper. Different switching states are combined with PWM control to produce and maintain a constant average output voltage despite the occurrence of converter open circuit and short circuit faults. The performance of the new fault tolerant circuit topology is analyzed in terms of power losses, efficiencies and output voltage harmonics. Experimental results obtained with a prototype 1 kW circuit have been presented to verify the proposed design and demonstrate the ability of the converter to achieve fault tolerant operation.

Appendix

TABLE V
FAULT TOLERANT INVISTIGATIONS IN THE DIODES

Switches	Actions	
	Open circuit fault	Short circuit fault
D1	Not involved in forward power flow operation.	Deactivate SE4 and activate SA1 and SE8
D2	Not involved in forward power flow operation.	Keep SE5 open.
D3	Not involved in forward power flow operation.	Keep SE6 open.
D4	Not involved in forward power flow operation.	Deactivate SE7 and activate SA2 and SE9
DA1	Not involved in forward power flow operation.	Deactivate SE8 and activate S1 and SE4
DA2	Not involved in forward power flow operation.	Deactivate SE9 and Activate S4 and SE7
D5	Change to different switching states combinations and D.	Deactivate SE1 and change to different switching states combinations and D.
D6	Not involved in forward power flow operation.	
D7	Not involved in forward power flow operation.	
D8	Change to different switching states combinations and D.	
D9	Change to different switching states combinations and D.	Deactivate SE2 and change to different switching states combinations and D.
D10	Not involved in forward power flow operation.	
D11	Not involved in forward power flow operation.	
D12	Change to different switching states combinations and D.	
D13	Change to different switching states combinations and D.	Deactivate SE3 and change to different switching states combinations and D
D14	Not involved in forward power flow operation.	
D15	Not involved in forward power flow operation.	
D16	Change to different switching states combinations and D.	

TABLE VI
FAULT TOLERANT INVISTIGATIONS IN THE POWER DEVICES

Switches	Actions	
	Open circuit fault	**Short circuit fault**
S1	Activate SA1 and SE8	Deactivate SE4 and activate SA1 and SE8
S2	Not involved in forward power flow operation.	Keep SE5 always open
S3	Not involved in forward power flow operation.	Keep SE6 always open
S4	Activate SA2 and SE9	Deactivate SE7 and activate SA2 and SE9
SA1	Activate S1 and SE4	Deactivate SE8 and activate S1 and SE4
SA2	Activate S4 and SE7	Deactivate SE9 and activate S4 and SE7
S5	Change to different switching states combination and D	Deactivate SE1 and change to different switching states combinations and D.
S6	Change to different switching states combinations and D.	Deactivate SE2 and change to different switching states combinations and D
S7	Change to different switching states combinations and D.	Deactivate SE3 and change to different switching states combinations and D.

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