Direct Measurement of MOSFET Channel Strain by Means of Backside Etching and Raman Spectroscopy on Long-Channel Devices

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***Abstract*—Measuring strain in long-channel MOSFETs on silicon-on-insulator (SOI) and strained-SOI platforms is demonstrated using ultraviolet (UV) Raman spectroscopy. Removal of the Raman inactive strain-inducing metallization layers is avoided by etching trenches under transistors without mask alignment in order to expose the channel region. The technique is shown to be repeatable and does not alter the initial strain state in the channel. The applicability of this technique to short-channel transistors is also discussed.**

***Index Terms*—Bosch, deep reactive-ion etching (DRIE), MOSFETs, Raman spectroscopy, silicon on insulator (SOI), strain, strained SOI (SSOI), strained silicon.**

I. Introduction

STRAIN has been playing a vital role in enhancing the performance of complementary-metal–oxide–semiconductor (CMOS) transistor technology since the 90-nm node. With the progressive reduction of transistor dimensions, the effect of strain on the electrical performance of a transistor becomes more critical. Therefore, quantifying strain within processed transistors is important in determining how strain can be engineered to continue enhancing transistor performance. To date, channel strain within processed transistors has either been predicted using finite-element modeling (FEM) [1] or, more recently, has been measured using high-resolution TEM (HRTEM) [2]. However, HRTEM is time consuming and requires complex computations and simulations. Moreover, it requires that the channel is adjacent to unstrained silicon having the same orientation, which might not be the case when channel orientation is engineered to achieve mobility enhancement. Strain measurements using Raman spectroscopy do not suffer from these drawbacks; however, metallization layers are Raman inactive. This means that transistors have to be deprocessed by removing the metallization layers before measuring channel strain using Raman spectroscopy. This could be a problem when metallization layers and nitride capping are used to induce strain in the channel. By removing them, the strain state in the channel is altered. In this letter, ultraviolet (UV) Raman spectroscopy is used to solve this challenge on silicon-on-insulator (SOI) and strained-SOI (SSOI) platforms by exposing transistors from the bottom by means of reactive-ion etching [3], thereby analyzing the channel strain without the need to remove the strain-inducing layers on top. The technique is demonstrated on long-channel transistors to ease the validation of the measured strain values, as short-channel transistors are known to experience some relaxation and, hence, high strain variability.

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II. Device Fabrication

Some 10-μm long channel NMOS transistors were fabricated on two different platforms; SOI and SSOI [4]. The SOI wafer was fabricated using the separation-by-implanted-oxygen (SIMOX) process, while the SSOI wafer was processed using wafer bonding and a donor wafer with Si biaxially strained to a $Si_{0.8}Ge_{0.2}$ strain-relaxed buffer or virtual substrate. The transistors were fabricated using a conventional CMOS process flow with 1.5-nm thermal silicon oxynitride gate dielectric, 100-nm polysilicon gate, and 25-nm elevated source/drain regions before highly doped drain formation and Ni silicidation. The two types of strain engineered in the NMOS channel are as follows: 1) SOI (uniaxial) with a 100-nm tensile nitride, strained contact etch stop layer (sCESL) having 800-MPa intrinsic stress and 2) SSOI (biaxial). The thickness of the Si channel was 15-nm, and the buried oxide was 150-nm.

III. Experimental Details

For the deep reactive-ion etching (DRIE) of the trenches, the sample (die, 2 cm $\times$ 1 cm) was first supported by sticking its top to another Si substrate with wax to prevent strain relaxation after sample preparation. Square trenches of 1.2 mm $\times$ 1.2 mm were then etched from the sample bottom after

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TABLE I
SETTINGS FOR THE BOSCH ETCH (DRIE)

SETTINGS	ETCH CYCLE	PASSIVATION CYCLE
Gas flow rate (sccm)	SF_6=450	C_4H_8=200
Power on coil (W)	3000	1000
Power on platen (W)	50	0
Pressure (mTorr)	20	40

mechanically thinning the sample substrate down to 100 μm [5]. The Si substrate was only thinned to 100 μm to prevent sample chipping during mechanical polishing. Then, 100-μm-deep trenches were randomly etched from the bottom of the die using a positive photoresist as an etch mask. The process was iterative as there was no guarantee that there will be transistors that can be analyzed within the etched trench. This eliminates the need for mask alignment. An STS advanced silicon etch tool was used to etch trenches through the bottom using the Bosch process [6]. The power applied to a coil generated the plasma. Periodic etch cycles using SF_6 gas, followed by passivation with C_4H_8 gas, were used. Passivation steps stopped lateral etching, resulting in vertical trench sidewalls. A 3-s etch cycle, followed by 2 s of passivation, resulted in about 8-μm/min overall etch rate. This was repeated all the way to the buried oxide, thus making the features visible through the trenches. Due to the large selectivity between etched Si and SiO_2 ($> 100 : 1$), it was possible to stop precisely at the buried oxide layer without significantly etching it. The sample was held on a platen cooled to 10 °C. Table I lists the settings for the etching and passivation cycles.

Raman spectroscopy measurements were taken with a Horiba Jobin Yvon LabRAM system fitted with UV laser (364 nm), with a penetration of ∼9–12 nm in Si [7], in order to make sure that only the channel was probed and not the polysilicon and sCESL layers on top. Peaks were fitted using Lorentzian/Gaussian peaks with peak fitting software. The laser power was about 0.7 mW at the sample surface (measured with a power meter) to prevent thermally induced peak shifts. Three line scans were taken across each measured transistor channel to show repeatability of measurement and to determine the error in the measured channel strain as a standard deviation expressed as a percentage of the strain median.

IV. RESULTS AND DISCUSSION

Fig. 1 shows the strain variation of three line scans across the 10-μm channel length with the optical image of the transistor through the DRIE trench shown in the inset. The measured strain agrees well with the theoretical value for $Si_{0.8}Ge_{0.2}$ (∼0.8%), which shows that strain is not compromised by etching trenches under transistors with biaxially strained channels. The strain medians of two biaxially strained transistor channels (10 μm long) on different dies are $0.8\% \pm 0.05\%$. This error could be due to material variability as a result of device fabrication. The agreement of the measured strain within the experimental error shows that the technique is repeatable even without any mask alignment.

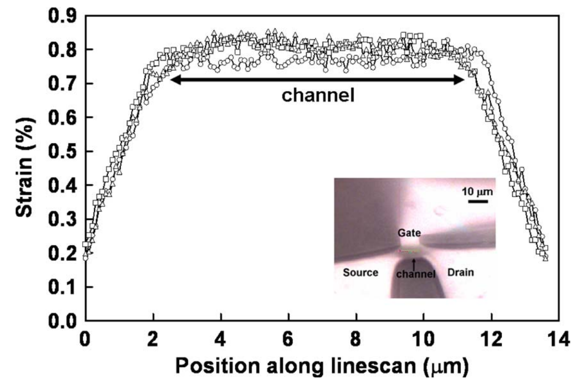

Fig. 1. Strain variation across a 10-μm channel of an SSOI transistor taken through trenches beneath the transistor. The SSOI channel was strained to $Si_{0.8}Ge_{0.2}$ (0.8% strain), which agrees with the measured channel strain. This shows that strain is not compromised by creating trenches underneath the transistors. The inset is the optical image of the transistor taken through the DRIE trench.

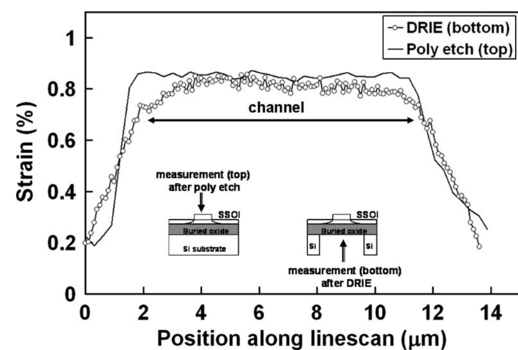

Fig. 2. Equal strain magnitude across 10-μm transistors, i.e., one etched from the top (poly etch) and the other from the bottom (DRIE), showing strain in the channel is not compromised by the sample preparation technique. Raman measurements were taken with UV laser. The inset is a schematic of the measurements taken from the top of the gate after poly etch and from the bottom of the gate after DRIE.

In order to experimentally confirm that the sample preparation process does not affect the measured strain magnitude within fabricated transistors, another sample was etched for 15 s in poly etch (HF/HNO_3) [8] to expose the gate area. The channel strain profiles extracted from line scans taken with UV laser across 10-μm channel transistors, i.e., one etched from the top (poly etch) and the other from the bottom (DRIE), are shown in Fig. 2. The inset in the figure shows the schematic of where the measurements were taken. As can be seen in Fig. 2, strain magnitudes agree within the experimental error, thus confirming that the measured channel strains are genuine and that sample preparation does not alter strain. The subtle difference in the strain profiles between the two measurements could be due to the absence of metallization layers in the poly-etched sample and, hence, why the strain profile rolls off faster at its channel edges.

The DRIE process was repeated on SOI transistors with sCESL capping in order to investigate if bowing in the channel occurs as a result of the sCESL on the top and the etching from the bottom. Fig. 3 is the strain variation of three line scans

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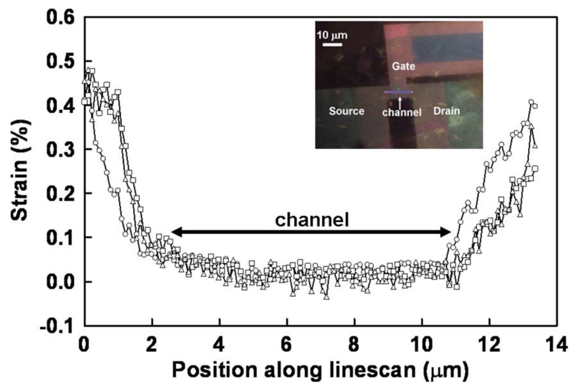

Fig. 3. Strain variation across a 10-μm channel of an SOI transistor uniaxially strained using sCESL. The absence of strain is due to the sCESL not having an effect on long channels. Strain measurements are taken through trenches beneath the transistor. The inset is the optical image of the transistor taken through the DRIE trench.

across the 10-μm channel length, and the inset is the optical image of the transistor through the trench after DRIE. The measured strain shows that the sCESL layer does not induce strain in the long channel [9], as expected, and also confirms that etching trenches under these transistors does not cause bowing in the channel. The channel (10 μm long) strain median of two SOI transistors with sCESL capping on different dies is $0\% \pm 0.05\%$. There is no strain induced in these transistors, as expected, which shows that the method is repeatable.

While this method is currently successful for long-channel transistors, it is a challenge for short-channel transistors as the channel length would be comparable to the measuring laser spot size ($\sim$500 nm). Heavy doping in the source and drain regions would contribute to the overall signal [10], thereby resulting in peak shifts that are not solely due to strain but also due to doping. The development of tip-enhanced Raman spectroscopy (TERS) [11], in addition to this backside etching technique, could enable strain mapping of channel dimensions in current technology nodes as the spatial resolution in TERS approaches about 20 nm. TERS is time intensive and lacks repeatability as it is in its early stages of development [12], [13]. It requires fresh tip preparation (coating), which depends on the laser wavelength to be used during Raman measurements. Standardization (e.g., tip coating material and enhancement calculation), repeatability, and authenticity of TERS enhancements are big challenges that are yet to be demonstrated. Also, getting TERS enhancements through the buried oxide layer needs to be investigated.

V. Conclusion

The feasibility of using Raman spectroscopy to measure channel strain within fabricated transistors has been demonstrated using long-channel devices on an SOI platform with sCESL capping and on an SSOI platform by etching trenches under transistors. Sample preparation has shown to not affect the strain state. The technique was shown to be repeatable even without any mask alignment required during the trench etching. The applicability of backside etching, in addition to the development of TERS, has a potential of mapping channel strain in current technology nodes.

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References

[1] G. Eneman, P. Verheyen, A. D. Keersgieter, M. Jurczak, and K. D. Meyer, “Scalability of stress induced by contact-etch-stop layers: A simulation study,” *IEEE Trans. Electron Devices*, vol. 54, no. 6, pp. 1446–1453, Jun. 2007.

[2] F. Hue, M. Hytch, H. Bender, F. Houdellier, and A. Claverie, “Direct mapping of strain in a strained silicon transistor by high-resolution electron microscopy,” *Phys. Rev. Lett.*, vol. 100, no. 15, pp. 156 602-1–156 602-4, Apr. 2008.

[3] P. J. M. Hopstaken, C. Cabral, D. Pfeiffer, C. Molella, and P. Ronsheim, “Towards routine backside SIMS sample preparation for efficient support of advanced IC process development,” *AIP Conf. Proc.*, vol. 1173, pp. 94–98, Sep. 2009.

[4] E. Augendre, G. Eneman, A. D. Keersgieter, V. Simons, I. D. Wolf, J. Ramos, S. Brus, B. Pawlak, S. Severi, F. Leys, E. Sleeckx, S. Locorotondo, M. Ercken, J.-F. D. Marneffe, L. Fei, M. Seacrist, B. Kellerman, M. Goodwin, K. D. Meyer, M. Jurczak, and S. Biesemans, “On the scalability of source/drain current enhancement in thin film sSOI,” in *Proc. ESSDERC*, Grenoble, France, 2005, pp. 301–304.

[5] R. M. B. Agaiby, “Nanometer scale strain characterisation using Raman spectroscopy,” Ph.D.dissertation, School Elect. Electron. Comput. Eng., Newcastle Univ., Newcastle upon Tyne, U.K., 2009.

[6] F. Laermer and A. Schilp, “Method of anisotropically etching silicon,” U.S. Patent 5501893, Mar. 26, 1996.

[7] J. Humilcek, M. Garriga, M. I. Alonso, and M. Cardona, “Optical spectra of Si_xGe_{1-x} alloys,” *J. Appl. Phys.*, vol. 65, no. 7, pp. 2827–2832, Apr. 1989.

[8] “MEMS exchange catalog,” Polysilicon Wet Etch. [Online]. Available: http://www.mems-exchange.org/catalog/P2226

[9] S. Orain, V. Fiori, D. Villanueva, A. Dray, and C. Ortolland, “Method for managing the stress due to the strained nitride capping in MOS transistors,” *IEEE Trans. Electron Devices*, vol. 54, no. 4, pp. 814–821, Apr. 2007.

[10] M. Chandrasekhar, J. B. Renucci, and M. Cardona, “Effects of interband excitations on Raman phonons in heavily doped n-Si,” *Phys. Rev. B, Condens. Matter*, vol. 17, no. 4, pp. 1623–1633, Feb. 1978.

[11] A. Tarun, N. Hayazawa, M. Motohashi, and S. Kawata, “Highly efficient tip-enhanced Raman spectroscopy and microscopy of strained silicon,” *Rev. Sci. Instrum.*, vol. 79, no. 1, pp. 013 706-1–013 706-10, Jan. 2008.

[12] L. Zhu, J. Atesang, P. Dudek, M. Hecker, J. Rinderknecht, Y. Ritz, H. Geisler, U. Herr, R. Geer, and E. Zschech, “Experimental challenges for approaching local strain determination in silicon by nano-Raman spectroscopy,” *Mater. Sci. Poland*, vol. 25, pp. 19–31, 2007.

[13] S. H. Christiansen, M. Becker, S. Fahlbusch, J. Michler, V. Sivakov, G. Andra, and R. Geiger, “Signal enhancement in nano-Raman spectroscopy by gold caps on silicon nanowires obtained by vapor–liquid–solid growth,” *Nanotechnology*, vol. 18, no. 3, pp. 035503-1–035503-6, Jan. 2007.

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