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Thermal atomic layer deposition was used to form ultra-thin interlayers in metal/interlayer/semiconductor Ohmic contacts on n-type and p-type Si. AlO_x of thickness 1–2 nm was deposited at 120 °C on Si substrates prior to metallization, forming Ni/AlO_x/Si contacts. Conductivity improved by two orders of magnitude but the contacts remained rectifying. When they were annealed at 200 °C, the conductivity increased by another order of magnitude and the samples became Ohmic. A minimum specific contact resistivity of 1.5×10^{-4} Ω-cm^2 was obtained for structures based on lightly doped (10^{15} cm^{-3}) Si substrates. Existing models that describe Fermi level de-pinning do not fully explain our results, which are however consistent with other experimental data in the literature. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4892003]

One of the near-term challenges for semiconductor-based technologies is developing low resistance Ohmic contacts.[1] Continued down-scaling has resulted in decreased contact area and a corresponding increase in contact resistance, R_{CO}, which can be described by[2]

$$R_{CO} = \frac{\rho_{CO}}{area} \propto \exp\left[\frac{\Phi_{SBH}}{\sqrt{(N_D)}}\right], \quad (1)$$

where ρ_{CO} is the specific contact resistivity, N_D is doping density, and Φ_{SBH} is Schottky barrier height. Because N_D is limited by the dopant's solubility in a semiconductor, the modulation of barrier height is key in the minimization of R_{CO} according to Eq. (1). Energetically, the Schottky barrier height can be considered to be the difference between the metal work function, ϕ_M, and semiconductor electron affinity, χ_S

$$\Phi^n_{SBH} = \phi_M - \chi_S, \quad (2)$$

$$\Phi^p_{SBH} = \chi_S - \phi_M + E_g, \quad (3)$$

where Φ^n_{SBH} and Φ^p_{SBH} represent the barrier height for n-type and p-type substrates, respectively.[3,4] This treatment assumes no interaction between the metal and semiconductor layers. Experimentally, the barrier height is often found to be almost independent of the metal work function.[5] This phenomenon is often attributed to a "pinning" of the Fermi level at some fixed energy within the band gap of the semiconductor. Several models have been developed to explain Fermi level pinning, including intrinsic effects, such as metal-induced gap states (MIGS)[6,7] or interface electric dipoles,[8] as well as extrinsic effects, such as interfacial atomic structure[9] and interface defects.[10] Several groups have sought to lower contact resistance by using ultra-thin interlayers between metal and semiconductor. Connelly *et al.*[11] showed that inserting an ultrathin layer of Si_3N_4 between metal and n-Si considerably lowers the contact resistance. Similar results have been demonstrated on Ge using Ge_3N_4,[12] TiO_2,[13] GeO_x, and AlO_x[14] interlayers. The technique was also demonstrated on III-V semiconductors by Hu *et al.*[15] The presence of fixed charges within interlayers has also been proposed to explain reduced contact resistance.[16] In separate studies, reductions in metal/interlayer/semiconductor (MIS) contact resistance have been reported on n-type and p-type 10^{15} cm^{-3} doped Si substrates. Coss *et al.*[17] used TaN electrodes and explained the improvement in contact resistance to p-type Si in terms of AlO_x/SiO_2 dipoles. They did not report results on n-type substrates, where this explanation would have predicted increased contact resistance. Agrawal *et al.*[18] used various metal electrodes, and explained the improvement in contact resistance to n-type Si in terms of reduced electron tunneling from the metal to MIGS in the semiconductor—they did not report results on p-type substrates where an increase in contact resistance would be predicted using their explanation.

In this Letter, improved contact resistance for Ni contacts to both n-type and p-type Si is reported, using ultra-thin interlayers of AlO_x grown by atomic layer deposition (ALD). While the results for individual n- or p-type substrates can be explained by the de-pinning of the Fermi level, in accordance to MIGS and/or dipole models, the paired results reported here would suggest that a different mechanism is responsible for the contact resistance reduction observed.

Lightly doped ($\sim 10^{15}$ cm^{-3}) n-type and p-type Si (100) substrates were used, both to emphasize the thermionic barrier and to make barrier height extraction more accurate via the electrical measurements. Substrate surfaces were prepared by a solvent clean, a "piranha" clean and an RCA clean finishing with two HF dip stages to remove native oxide. Ultrathin AlO_x layers were deposited on the prepared substrate surfaces by thermal ALD using an Oxford Instruments Flex Al reactor, with adduct-grade trimethylaluminium (TMA) and H_2O as precursors. For the test specimens, layers were deposited over a range of thicknesses at a deposition temperature of 120 °C with pulse/purge times of 0.2/1.5 s and 0.2/6 s for TMA and H_2O, respectively. The precursors were supplied to the chamber by vapor draw.

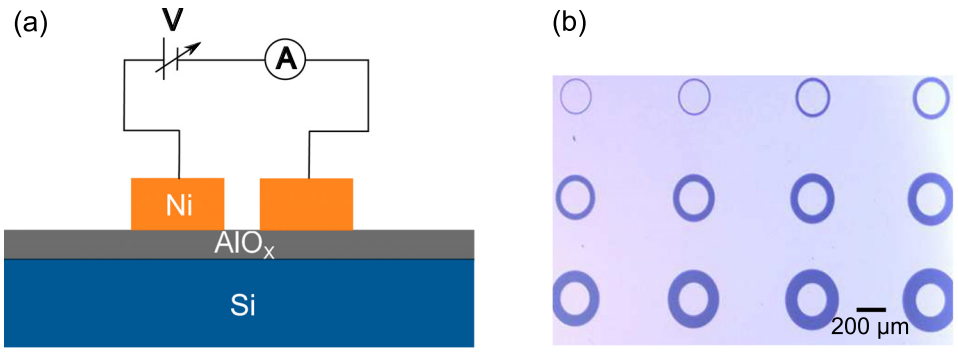

FIG. 1. (a) Geometry of back-to-back diodes with different areas varying between 7×10^{-4} cm^2 and 12×10^{-4} cm^2. (b) Optical microscope image of CTLM structures used to measure contact resistance.

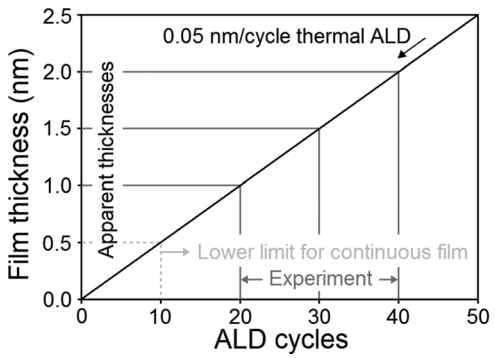

FIG. 2. Schematic thermal ALD AlO_x deposition rate. The range of cycles used in the experiments, and the apparent resulting film thicknesses are sketched.

Contacts were formed with 70 nm-thick Ni films deposited by e-beam evaporation to form a metallization layer (Fig. 1(a)). This layer was patterned using lift-off to create circular contacts with different surface areas. Circular transmission line measurement (CTLM) structures[19] (Fig. 1(b)) were fabricated on the same samples to determine the contact resistance. Our sample transfer length (30–40 μm) and contact resistance ($\sim 10^{-4}$ Ω-cm^2) are large enough for the CTLM technique to be applicable. Control Ni/Si samples were produced without AlO_x interlayers. Electrical transport measurements were carried out using back-to-back Schottky contacts. Under both positive and negative bias, only the reverse current is measured. This eliminates large contributions from series resistance due to the lightly doped substrates. Moreover, changes in the measured effective barrier height Φ_B (Eq. (4)), are most clearly observed by changes in reverse current. The series resistance was measured in the Ni/Si devices by depositing a back contact. It was found to be ~396 Ω at room temperature by using the Werner method. This high series resistance causes drastic curvature of the forward J-curve even at low voltages, which makes data analysis for the extraction of barrier height difficult. The ideality factor was calculated by correcting the J-V data for the extracted resistivity. The extracted value for n is 1.088.

Fig. 2 depicts the thickness/cycles relationship for thermal ALD AlO_x films. Relatively thick films (10 s–100 s of nm) using different numbers of cycles were deposited by ALD and their thicknesses measured by spectroscopic ellipsometry. The measurements were corroborated with step-etched atomic force microscopy measurements. From these data, the thermal ALD growth rate is estimated to be ~0.05 nm/cycle, which is the diagonal line on the figure. An ALD AlO_x deposition of at least 10 cycles is necessary to form a continuous layer, below which an island growth mechanism is seen.[20] For this study, AlO_x interlayers were grown using 20, 30, and 40 ALD cycles, corresponding to film thicknesses of 1, 1.5, and 2 nm. Our experiments operate just over the minimum cycle limit for a continuous layer and it is difficult to get accurate film thickness measurements at these dimensions. As such we have referred to cycles, rather than physical thicknesses, throughout. Fig. 3 shows J-V characteristics for Ni/AlO_x/Si contacts as a function of AlO_x thickness at room temperature. All the samples exhibited non-linear J-V characteristics. While the reverse saturation current density is low for the control Ni/Si contacts, an enhancement greater than two orders of magnitude is noted for Ni/AlO_x/Si contacts. This increase in reverse current density corresponds with a reduction of the effective barrier height. Effective barrier heights at room temperature were determined from the saturation current density, J_s, which is estimated by linear extrapolation of ln(J) vs V to zero voltage. Assuming a Richardson constant of $A^{**} = 112 \frac{A/cm^2}{K^2}$ for n-type Si and $32 \frac{A/cm^2}{K^2}$ for p-type Si,[21] the barrier height can be calculated using[22]

$$\Phi_B^{n,p} = \frac{kT}{q} ln \frac{A^{**}T^2}{J_s}, \tag{4}$$

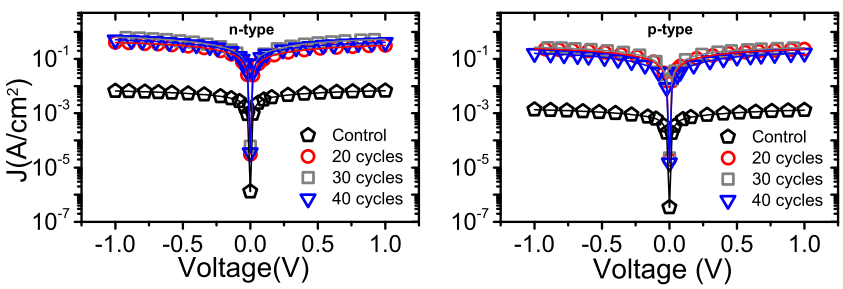

FIG. 3. J-V curves for Ni/AlO_x/Si test structures on n-type (left) and p-type (right) substrates for three AlO_x interlayer thicknesses and control Ni/Si samples.

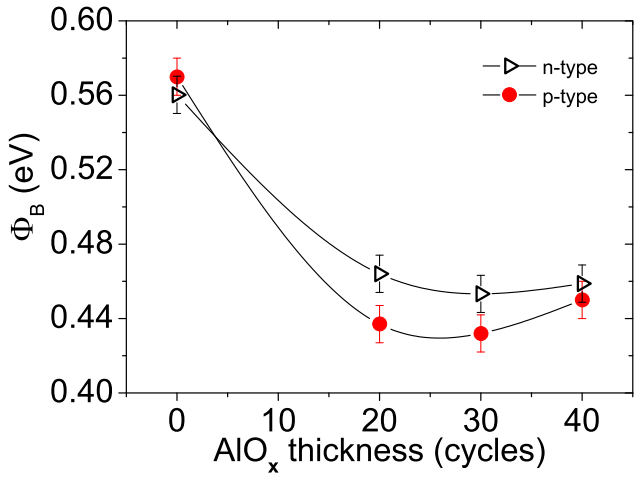

FIG. 4. Effective barrier heights extracted from J-V data for Ni/AlO$_x$/Si test structures on n-type and p-type substrates for three AlO$_x$ interlayer thicknesses and control Ni/Si sample (0 cycles). The trendline is for representation only.

where k is the Boltzmann constant, q is charge, and T is temperature. The effective barrier heights are plotted as a function of AlO$_x$ thickness in Fig. 4. $\Phi_B^n = 0.56$ eV is extracted for Ni/n-Si and $\Phi_B^p = 0.57$ eV for Ni/p-Si. These compare well with the reported values for Ni-n/p-Si barrier heights (cf. ~0.69/0.5 eV) in the literature.[23] Summing $\Phi_B^n + \Phi_B^p$ gives a value close to the band gap (E_g) of Si, providing additional confidence in our measurements. This result implies that the Fermi level is close to the mid-gap of Si in both n-type and p-type Ni/Si structures. The effective barrier height Φ_B^p sharply reduces to ~0.44 eV for a MIS sample with an AlO$_x$ interlayer of 20 cycles followed by a more gradual decrease as the interlayer gets thicker, exhibiting a minimum for an interlayer thickness of 30 ALD cycles. However, a similar trend is also seen for the n-type contacts, as shown in Fig. 4. The effect is slightly less pronounced for n-type contacts, with a more gradual decrease as the interlayer thickness increases. Effective barrier reductions of ~30% and ~20% are obtained for n-type and p-type MIS contacts, respectively. It is noted that the relation $E_g \approx \Phi_B^n + \Phi_B^p$ from Eqs. (2) and (3) does not hold for the MIS contacts reported in this study. Since our fabrication process is identical for both n- and p-type diodes, existing models used to explain Fermi level de-pinning would predict enhancement on either n- or p-type substrates, but not both. Effectively, the data in Refs. 17 and 18 support our premise despite using different interlayers and concentrating on one half of the energy distribution in each paper. Our minimum reported value of Φ_B (~0.43 eV) on p-type substrates compares well with the value of about 0.4 eV reported by Sinha *et al.*; albeit using heavily doped substrates and 500 °C anneal to form nickel silicide in their case.[24] The value we report here is specifically for the samples before heat treatment.

Fig. 5 shows the J-V characteristics at room temperature of Ni/Si and Ni/AlO$_x$/Si structures after annealing at 200 °C for 5 min. The MIS contacts changed from exhibiting rectifying to Ohmic behavior, while the metal/semiconductor (MS) contacts remained rectifying. The insets plot the same control data for n- and p-type structures on a reduced linear scale, to confirm their rectifying properties remain after the heat treatment. This indicates that different transport mechanisms are now taking place for MS and MIS structures. Temperature dependent J-V measurements from room temperature (27 °C) to 127 °C were later carried out on heat treated samples (measurements not shown). The weak temperature dependence of J-V for MIS contacts indicates thermionic emission is no longer the dominant transport mechanism, whereas thermionic emission remains in the case of the MS contacts. After annealing the contact resistance has improved by around an order of magnitude for the MIS contacts and is almost independent of interlayer thickness. A minimum specific contact resistivity ρ_{CO} of 1.5×10^{-4} Ω-cm^2 was obtained.

One explanation is that due to the diffusion of Ni into AlO$_x$ an intermixed dipole layer is formed. This kind of intermixing is possible at the very early stage of metal deposition on ultra-thin interfacial layers.[25] Several models have been proposed to explain the origin of this dipole effect, such as oxygen vacancies caused by substitution of dopant metal atoms in high-κ dielectrics,[26] average dipole moment of bonds at the interface,[27] and group electronegativity of dopant parent metals in the dipole layer.[28] The dipole sets up a large electric field close to the Si interface causing a sharp increase in the band bending of the Si majority carrier band. This will reduce the barrier width causing an increase in the probability of tunnelling of majority carriers, thus lowering the effective barrier height[29,30] (Fig. 6). Sinha *et al.*[24] and Koh *et al.*[31] have reported the tuning of SBH at NiSi/p-Si junction by the introduction of Al using ion implantation and its segregation after silicidation. They attributed this effect to the higher probability of holes tunnelling through a thin barrier. This narrowing was attributed to the electric field induced by impurity Al atoms.

In summary, a reduction of contact resistance is observed on both n- and p-type Si substrates using Ni/AlO$_x$/Si contacts. Existing models for Fermi level de-pinning do not fully describe these results. A 200 °C heat treatment

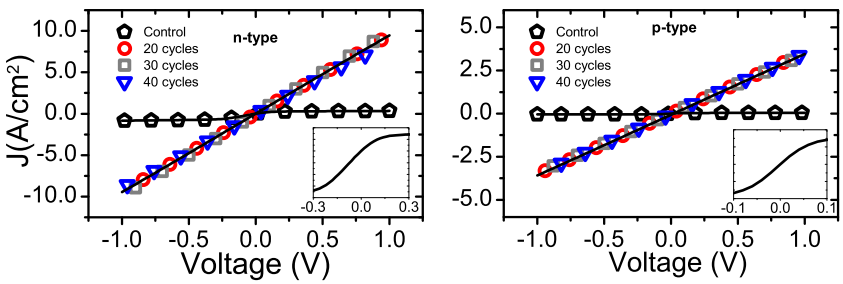

FIG. 5. J-V curves of heat treated contacts n-type (left) and p-type (right) substrates shown in linear scale. Ni/Si (Control) samples remained rectifying while those with interlayers changed from rectifying to Ohmic behavior. Insets show control sample measurements on a smaller scale (arbitrary y-axis, linear scale) which still show rectifying behavior.

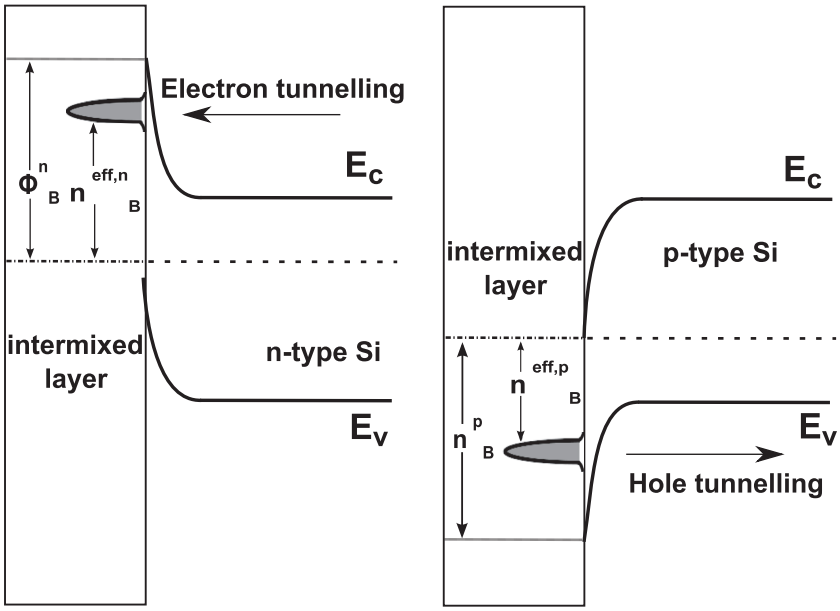

FIG. 6. Schematic band diagram showing the narrowing of the barrier width, and enhancement of the majority tunnelling current (in the case of n- and p-type substrates), due to the dipole-induced electric field.

results in Ohmic contacts for the MIS structures on n- and p-type Si. The control MS samples do not switch to Ohmic behaviour after the 200 °C anneal. This suggests that the anneal may give rise to metal migration and material changes in the AlO_x which act to suppress the effective Schottky barrier height, independent of doping.

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