Reliable Fabrication of Sub-10 nm Silicon Nanowires by Optical Lithography

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Abstract

The reliable and controllable fabrication of silicon nanowires is achieved, using mature CMOS technology processes. This will enable a low-cost route to integrating novel nanostructures with CMOS logic. The challenge of process repeatability has been overcome by careful study of material properties for processes such as etching and oxidation. By controlling anisotropic wet etching conditions, selection of nitride mask layer properties and sidewall oxidation, a robust process was achieved to realize silicon nanowires with sub 10 nm features. Surface roughness of nanowires was improved by a suitable oxidation step. The influence of process conditions on the shape of the nanowire was studied using TCAD simulation.

1. Introduction

Silicon nanostructures are important components in applications such as biosensors [1],thermoelectric devices [2, 3], solar cells [4, 5] and biomedical recording [6-8]. Moreover, silicon nanowires at dimensions below 10 nm have attracted considerable attention for use as building blocks in next generation of nanoelectronic devices, such as single electron devices and quantum devices [9-11].
Recently, several groups have reported the fabrication of very fine nanostructures without using high resolution patterning [12-14]. Such an approach would allow the integration of nano-scale devices with more mature CMOS technology. These methods typically begin with the patterning of wide structures using standard lithography, as shown for our devices in figure 1. This is followed by other processes such as dielectric (e.g. silicon nitride) deposition for masking, thermal oxidation and etching, including anisotropic wet etching. In this way, the fabrication of sub-10 nm structures is possible from microstructures defined by standard lithography. This can be categorized as an indirect method because the final nanostructure is not identical to the patterned one. However, previously reported studies do not discuss the main challenges in these fabrication methods, nor the fundamental issues that control the reproducibility of the process, quality of the fabricated devices and the control of nanowire dimensions to achieve sub 10 nm nanowires.

In this paper, the silicon nitride deposition and removal were studied by depositing several silicon nitride films using plasma-enhanced chemical vapor deposition (PECVD) and radio frequency (RF) sputter. Their optical properties were studied before and after thermal oxidation. It is well known that the annealing of silicon nitride in oxygen ambient affects its properties where the nitride film starts to convert to silicon dioxide/oxynitride [15, 16]. Moreover, the oxidized silicon nitride film has different etching properties compared with the as-deposited one. Previous studies have paid little attention to the effect of the properties of silicon nitride on the reproducibility of

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the process, yet controlling these properties and the silicon nitride and oxide thicknesses is crucial for successful fabrication.

A series of experimental measurements were performed on TMAH and KOH to find out which can best obtain a reproducible process with high control of the etching profile. The anisotropic wet etching of silicon using TMAH and KOH has been employed to realize many silicon nanostructures. Both etchants have similar etching characteristics. KOH has excellent anisotropic properties and high etching selectivity over <111> Si and it can obtain a smoother sidewall, while the TMAH etchant is non-toxic and it does not contain alkaline contaminants. Moreover, it offers high etch selectivity against silicon dioxide in comparison with KOH. It is crucial to choose the appropriate etchant and optimize the etch conditions as this will have a significant effect in controlling the thickness of the nanowire as well as the quality of their surfaces. The fabrication of sub-10 nm nanowires is also described in this paper.

Finally, the morphology of nanowire surfaces with different etching conditions as well as after thermal oxidation treatment is also investigated in this work. The surface morphology of the fabricated structure is determined by fabrication conditions: mainly etching and thermal oxidation. In particularly, parameters such as electrical and thermal resistivities and optical loss are directly related to surface roughness.

2. Methods

2.1. Fabrication of nanowire devices

Figure 1 illustrates the fabrication of nanowires at precise locations without high resolution patterning [14]. A 30 nm oxide was thermally grown on <100> SOI substrates. Optical lithography was then used to define the location for the formation of nanowires. A buffered oxide etch (BOE) was used to open a window through the oxide. A layer of silicon nitride of thickness 30 nm was deposited using the RF sputter in pure N_2 at 90 °C. Then, the nitride film was patterned in another lithography step where the exposed silicon nitride was etched using BOE, as shown in figure 1(a). A 25%wt TMAH solution with added 7.5% IPA at 56 °C was utilized to etch the exposed silicon. Due to the anisotropic characteristics of TMAH etching, the etch stops at the <111> plane and produces an angle of 54.7° with the <100> plane (figure 1(b)). The wafer was oxidised to protect the exposed <111> plane for the next anisotropic etching step. During sidewall oxidation, not only was silicon oxidised, but also the silicon nitride was partially oxidized (figure 1(c)). The top layer of oxidized silicon nitride film was removed using an ion milling step in pure argon (Ar), which was followed by the use of boiling phosphoric acid to remove the silicon nitride layer (figure 1(d)). Another step of 25%wt TMAH solution with added 7.5% IPA at 56 °C was performed to define the nanowires. The nanowires were then immersed in BOE for a few seconds in order to remove the sidewall oxide (figure 1(d)).

2.2. Silicon nitride preparation and characterisation

Different silicon nitride types were deposited on silicon substrate under different conditions using PECVD and an RF magnetron sputter. The RF silicon nitride films were deposited under different gas mixtures of pure Ar, pure N_2 and 5:1 Ar/N_2. The deposition temperature for the RF silicon nitride was at 90 °C with 150 W power and a pressure of 10 mtorr. Film thicknesses were between 55 nm and 75 nm. The optical properties of the silicon nitride were analyzed using spectroscopic ellipsometry at a wavelength of 633 nm. The silicon nitride films were annealed in oxygen at 930 °C for 35 min to study the influence of oxidation on their properties. Boiling phosphoric acid at about 165 °C and ion milling were used to etch the oxidized SiNx, and the etch selectivity over silicon dioxide was determined using ellipsometry.

Two models were used to analyse the properties of oxidised nitride film. First, the Bruggeman effective medium approximation was used to determine the volume fraction of silicon dioxide and effective refractive index of the medium. The effective refractive index of the medium n_{eff} was measured, and then the relative volume fraction of oxide f_{SiO_2} and nitride $f_{Si_xN_y}$ in the film were estimated approximately using the following equations [17, 18]:

$$f_{SiO_2}\frac{n_{SiO_2}^2 - n_{eff}^2}{n_{SiO_2}^2 + 2n_{eff}^2} + f_{Si_xN_y}\frac{n_{Si_xN_y}^2 - n_{eff}^2}{n_{Si_xN_y}^2 + 2n_{eff}^2} = 0 \qquad (1)$$

$$f_{SiO_2} + f_{Si_xN_y} = 1 \qquad (2)$$

where $n_{Si_xN_y}$ and n_{SiO_2} are the measured refractive indices of the as-deposited nitride film and the refractive index of silicon dioxide respectively.
A multi-layer model of the four phases SiO_2/SiOxNy/SiNx/Si was used to find the ratio of converted oxynitride and silicon dioxide thicknesses on silicon nitride to the total oxide thickness on the silicon substrate. In this model, the refractive index and thickness of the SiNx layer were known, while fitting parameters were used to determine the thicknesses of SiO_2 and SiOxNy. The SOPRA WINELLI II software was employed to analyse and simulate the ellipsometry data. The modified Cauchy-Lorentz dispersion law model was applied to the silicon nitride and oxynitride layers [19, 20].

2.3. Characteristics of TMAH and KOH

Three types of etching solutions were used to conduct the anisotropic wet etching experiments: 40 %wt KOH, 25 %wt TMAHC and 15.6 %wt TMAH, all at 56 °C with 7.5 % IPA added. The experiments were performed in open beakers with no stirring and with no samples placed in solution for more than 25 min.

2.4. Surface roughness extraction

The surface roughness of nanowires was characterised using AFM. The image was then processed using two steps of analysis, namely image levelling and root mean square roughness. Details of this technique are discussed elsewhere [21].

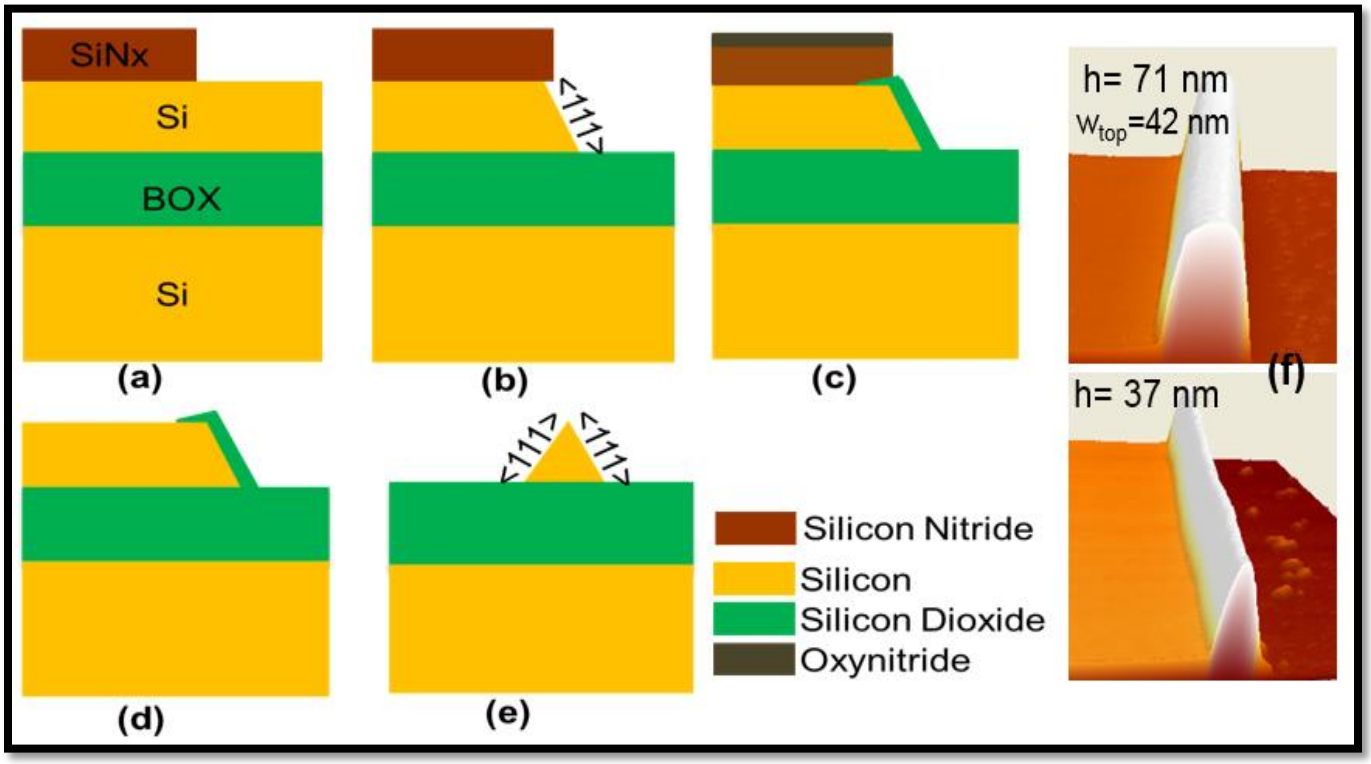

Figure 1. (a)- (e) Schematic shows the process steps for the fabrication of silicon nanowire. (f) 3D images of silicon nanowires with a trapezoidal cross-section (top); 3D images of silicon nanowires with a triangular cross-section (bottom).

3. Results

3.1. Nanowire profiles

The geometry of the fabricated nanowires was analysed using two types of non-contact AFM tips: very sharp SSS-NCHR tips with a typical tip radius of <5 nm and an aspect ratio of 4:1 at 200 nm; and commercial ACTA

tips with a typical tip radius <20 nm and aspect ratio of 1.5-3:1. The AFM profile of the type of nanowires fabricated in this process is shown in figure 1(f).

The limitation of an AFM is that its lateral resolution depends on the size and shape of the AFM tip, which makes the measured lateral AFM image wider than the actual structure. This is referred to as a convolution effect (see figure S1). Therefore, the increase in width due to the convolution effect was estimated by using a simple model that takes into account the diameter of the tip and the thickness and sidewall angle of the nanowire. The actual width of nanowire w as a function of the measured value w_m and the geometry of the nanowire and tip radius can be rewritten as:

$$w = w_m - 2i = \begin{cases} w_m - 2(\sqrt{R^2 - (R-h)^2} - h\cot\beta), & h_c \le R(1-\cos\beta) \\ w_m - 2(R\cos(90-\beta)) \quad , & h_c > R(1-\cos\beta) \end{cases} \qquad (3)$$

where R is the tip radius, h is the thickness of the nanowire and β is the sidewall angle of silicon, i is the increase in width, h_c is the critical thickness of nanowire (see supplementary information, figure S1).

To confirm the validity of the model, SEM and AFM images of nanowires were compared. AFM measurements were performed using a commercial ACTA tip. The measured width of the nanowire using AFM was about 123 nm (figure 2(a)), while the true width measured using an SEM image was 96 nm (figure 2(b)). Direct comparison between the two profiles indicates that the increase in width due to the convolution effect is 27 nm. This is equivalent to tip radius of R ~16 nm. This value of tip radius is realistic considering the degradation of the tip after using it for several scans.

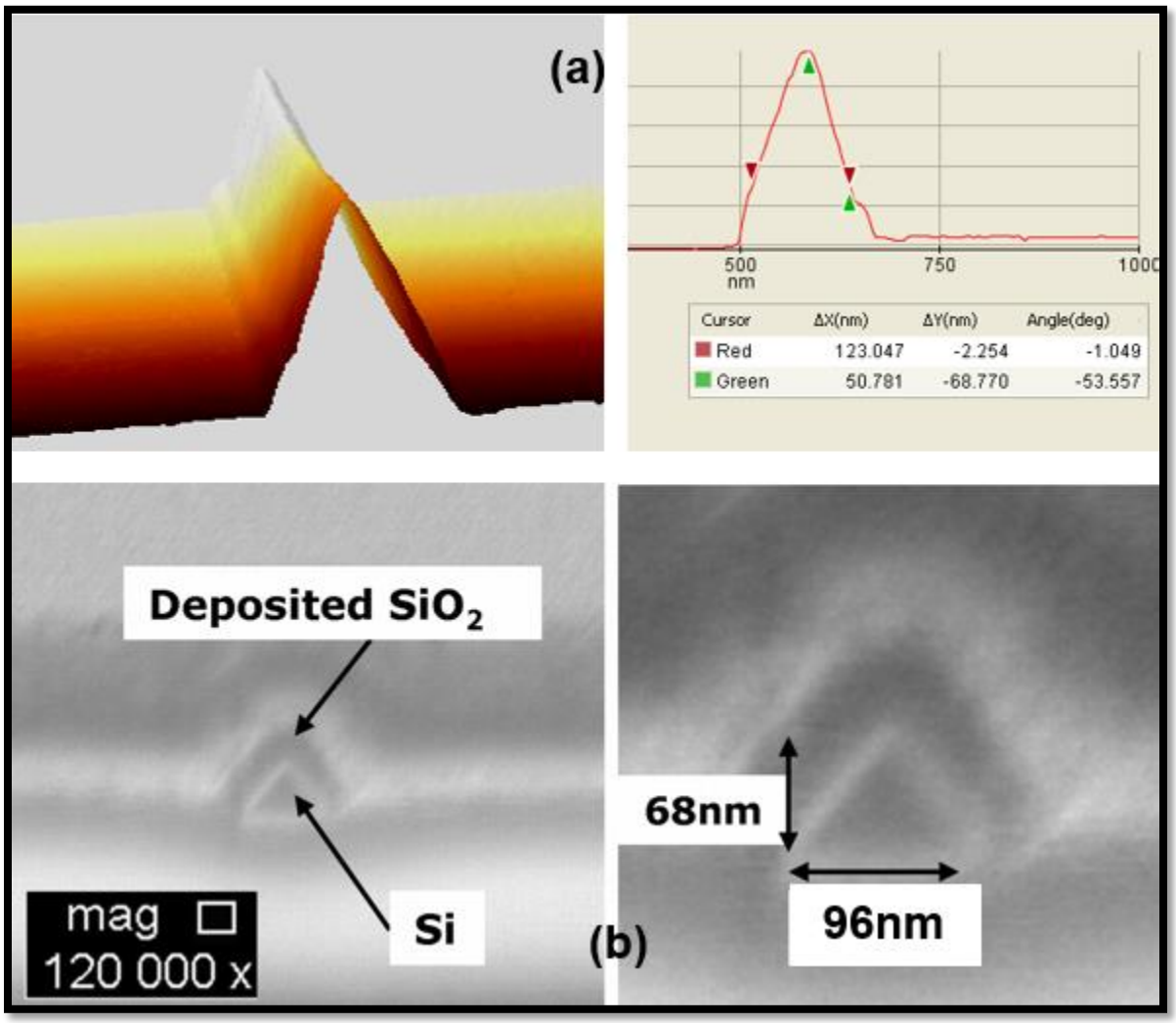

Figure 2. (a) AFM image of the silicon nanowire and its profile, (b) Measured the cross-section of the nanowire with SEM.

3.2. Optimization of sidewall oxidation for nanowire fabrication

As shown in the AFM image in figure 1(f), the fabrication process can yield nanowires with either trapezoidal or triangular cross-sections. The trapezoidal cross-section arises due to the lateral diffusion of oxygen under the edge of the silicon nitride layer during sidewall oxidation, figure 1(c), resulting in a so-called bird's beak structure. The lateral oxidation length is affected by several factors including nitride thickness, oxide underneath the silicon nitride, oxidation time and temperature, and the position of the nitride mask [22].

The experimental results show that lateral oxidation is also affected by the duration of the first anisotropic etch, figure 1(b). Figure 3(a) shows the AFM profile for two samples placed for 3 and 7 mins in KOH at 56 °C during the first wet etching step. The top width of the nanowire is seen to be about 85 nm for the sample after etching for 3 mins, but this is reduced to about 35 nm when the etching time increases to 7 mins. As the etching time increases, this leads to an increase of undercut. The increase of undercut results in a shorter birds's beak length, due to the fact that larger undercut improves the sealing between the silicon/silicon nitride interfaces, making it difficult to lift-up the nitride layer [23].

The effect of undercut on lateral length was further investigated by two-dimensional process simulation, using the TCAD Sentaurus simulator from SYNOPSYS (www.synopsys.com). The simulation was used to investigate the sidewall oxidation of silicon taking into account the deformation of silicon, diffusion of the oxidant species and the viscosities of the oxide and nitride layers. An oxidation step was simulated at 930 ºC for a relatively short time in order to grow an oxide of about 18 nm thickness on <100> silicon. A 0.5 nm layer of oxide was also inserted between the silicon and the silicon nitride layer to represent the native oxide that can be formed due to the exposure of silicon to air prior to nitride deposition. Figures 3(b) & 3(c) show that the bird's beak length is reduced with the increase in undercut. The bird's beak length was 12 nm for an undercut of 10 nm compared to 54 nm for no undercut.

Figure 3(d) illustrates the simulation results for the impact of nitride thickness. A thicker nitride mask results in shorter lateral oxide, due to the thick nitride layer strengthening the sealing to silicon compared with a thin layer which allows smaller deformation and a reduced oxidation window.

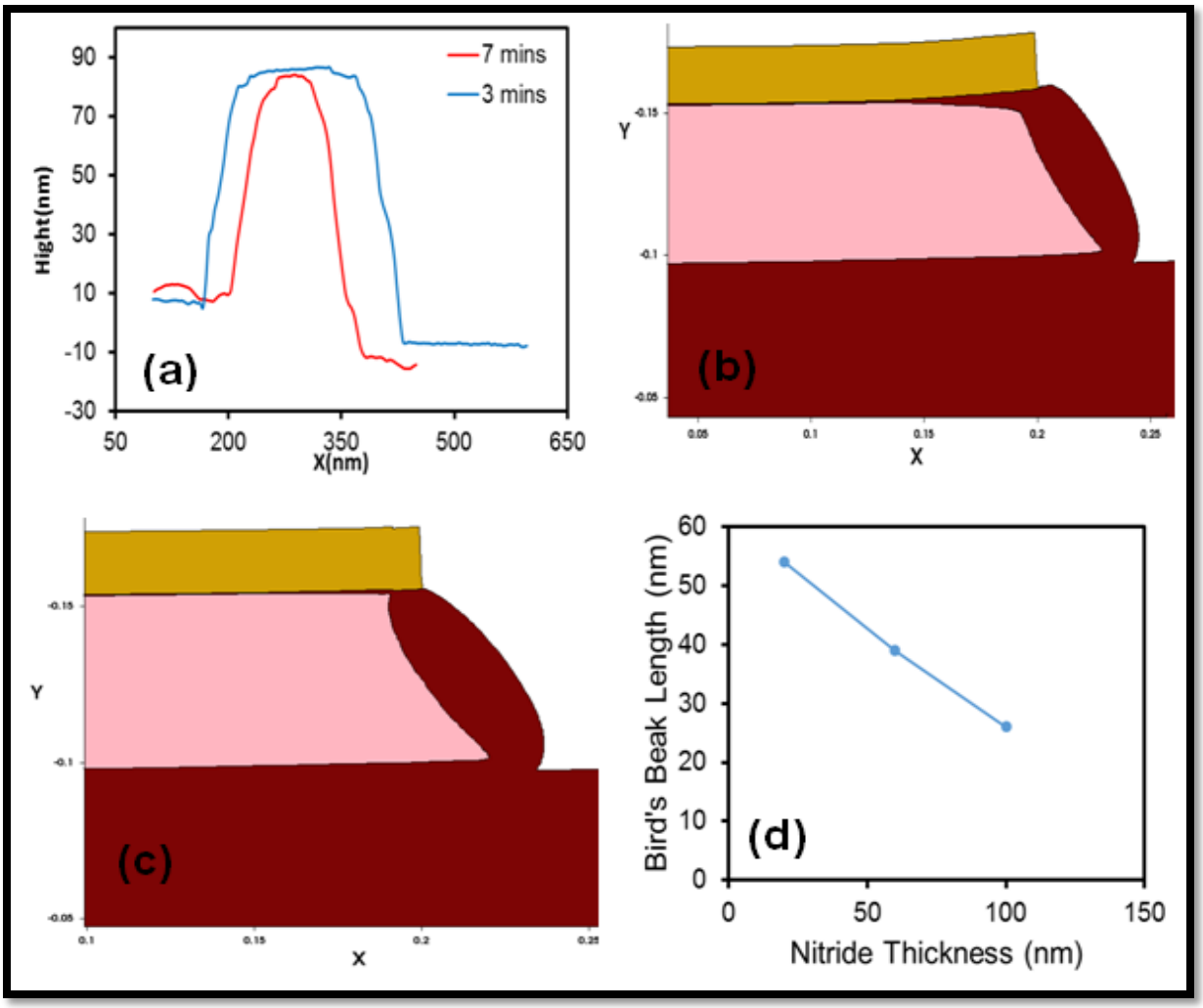

Figure 3. (a) Nanowire width at different 1st anisotropic etching times (2nd etching time was adjusted for 4 mins), (b) 2D simulation of sidewall oxidation of silicon with undercut undercut of 0 nm, (c) 2D simulation of sidewall oxidation with undercut of10 nm, (d) Effect of nitride thickness on bird's beak length.

3.3. Characterisation of silicon nitride films

The average refractive indexes of as-deposited nitride using RF sputter in pure Ar, 5:1 Ar:N_2 and pure N_2 are 2.37, 2.04 and 1.90 respectively. The refractive index of RF nitride films is reduced with increasing nitrogen ratio, and for deposition in pure N_2 the refractive index is about 1.9, which corresponds to Si_3N_4 given that:

$$n = 1.35 + 0.74\frac{Si}{N} \qquad (4)$$

As illustrated in table 1, all nitride films were affected by thermal annealing, clearly shown by the change of refractive index. The data in table 1 shows that the silicon-rich silicon nitride film (sputtered in pure Ar) has the thinnest oxide on top, where the oxidation rate was about 75 times lower than that of silicon, the oxide thickness on the silicon substrate was 21 nm, and approximately three times slower than that of the nitrogen-rich film (sputtered in pure N_2). However, the oxynitride thickness on a silicon-rich nitride is higher than the thickness of oxide grown on a silicon substrate, while it was about 23% of this thickness on the nitrogen-rich silicon nitride film as shown in table 1. The higher oxidation rate of silicon-rich silicon nitride compared with the nitrogen-rich silicon nitride can be ascribed to the presence of the high concentration of silicon in silicon-rich silicon nitride film. This makes the nitrogen-rich silicon nitride a better mask for thermal oxidation.

3.3.1 Etching of oxidized silicon nitride

The etch behavior of oxidized silicon nitride using phosphoric acid was observed to correlate with material type. It started with a very slow etch rate, which then increased until it reached approximately a constant value when the silicon nitride was exposed. Thus, etching the film with boiling phosphoric acid alone is inadequate, especially for a process that requires etching selectivity over silicon dioxide. Therefore, two etching steps were used: the first to remove oxynitride using RIE in pure argon (Ar); the second after the removal of the oxynitride layer involving etching in boiling H_3PO_4 which is the main etchant of silicon nitride.
Table 2 shows that the nitrogen-rich film has the highest etch selectivity over thermally grown oxide. Oxide thickness was measured by ellipsometry measurements, each obtained after 3 min etching with 6 etching periods. From the results it is clear that a nitrogen-rich film has the highest resistance to thermal annealing and can act as an effective mask during the sidewall oxidation.

Table 1. The ratios of oxynitride and oxide thicknesses on oxidized silicon nitride to the silicon dioxide thickness on bare silicon

		RF sputter pure Ar	RF sputter 5:1 Ar: N_2	RF sputter pure N_2	PECVD
Refractive index	As-deposited	2.37	2.04	1.90	1.94
	After annealing	1.67	1.57	1.55	1.61
Average $\frac{SiO_2 \text{ on } SiN_x}{SiO_2 \text{ on bulk Si}}$ %		1.3	2.3	3.6	3.2
Average $\frac{SiN_xO_y \text{ on } SiN_x}{SiO_2 \text{ on bulk Si}}$ %		104	57	23	22

3.3.2 Silicon nitride selection for nanowires process

During the removal of the nitride mask, the silicon dioxide at the sidewall is removed as well. Therefore, in order to ensure there is sufficient oxide remaining at the sidewall during the 2nd wet anisotropic etch step, the maximum silicon nitride thickness must be determined. The oxynitride thickness and the etching selectivity of the silicon nitride over silicon dioxide are key parameters which determine the maximum thickness of the nitride mask. The maximum thickness of the nitride mask is given by:

$$t_{max} = S_{SiN_x/SiO_2}(t_{ox} - t_R) \quad (5)$$

where S_{SiN_x/SiO_2} is the etching selectivity of silicon nitride after the removal of oxynitride over silicon dioxide in the phosphoric acid (H_3PO_4), which was the etchant used in the current experiments; and t_{ox} is the maximum oxide thickness that can be removed from the sidewall without causing a failure during the subsequent etching step, given by:

$$t_{ox} = t_{tot} - t_m \quad (6)$$

where t_{tot} is the oxide thickness grown on the sidewall and t_m represents the minimum oxide thickness at the sidewall required to act as a robust mask during the 2nd anisotropic etching step, the value of which was determined during experimental measurements and found to be 3 nm; t_R is the thickness of oxide consumed during the etching of oxynitride and oxide on the nitride film. It also indicates that the

ratio of silicon dioxide and oxynitride affects the nanowire process. A thicker oxynitride layer increases t_R(as shown in tables 1 & 2). Consequently an oxynitride layer that is too thick will result in the complete removal of sidewall oxide and failure in the formation of nanowires. Values of S_{SiN_x/SiO_2} for different films and t_R are shown in table 2. The maximum thickness of the silicon nitride mask for each type of silicon nitride material is provided in supplementary information (figure S2). Some experimental data are plotted, which are in agreement with predictions, where about 25% of the total silicon dioxide was removed during the ion milling step for all films followed by boiling phosphoric acid. These results show that nitrogen-rich silicon nitride is the most suitable to be used as a mask during sidewall oxidation for nanowire fabrication.

Table 2. Etch selectivity of oxidized silicon nitride over silicon dioxide in boiling H_3PO_4 and oxide thickness ratios consumed during the removal of oxide and oxynitride layers

Silicon nitride film	Etching Selectivity over SiO_2	(t_R) the average oxide consumption during SiO_2/SiO_xN_y removal
Pure Ar	3.4	$0.65t_{tot}$
Mixed Ar/N_2	3.7	$0.35t_{tot}$
Pure N_2	4.8	$0.25t_{tot}$
PECVD	5.6	$0.2t_{tot}$

3.4. Characterization of surface roughness

As the nanowires are formed by two anisotropic wet etching steps in addition to a thermal oxidation step, the quality of the nanowire surfaces is examined as a function of etching time and conditions. Although low TMAH concentration at high temperature offers a high etch rate, higher concentration offers a smoother surface. TMAH 25% was utilised with added 7.5 IPA at 56 °C to further improve the smoothness of the surface. The surface was investigated after different etching times and compared with the surface profile after the samples were oxidized at 930 ˚C to grow about 18 nm silicon dioxide. Figure 4(a) shows a dependence of rms roughness on etching time. Surface roughness increases by a factor of three after 20 mins etching time compared with 8 mins. However, a high rms roughness was observed when the etching time was too short (30 sec). It is expected that the <111> plane was not completely exposed after a short etching period instead other exposed planes start to be etched before reaching the <111> plane [24, 25]. Therefore, this suggests that the etching time should be long enough to expose the <111> plane and to obtain a stable result, but not too long so as to ensure obtaining a smooth surface.

The impact of thermal oxidation on rms surface roughness was also studied, which was significantly improved after annealing. An improvement in surface roughness after thermal oxidation was also observed for the <111> nanowire surface. The AFM image in figure 4(b) shows the sidewall of a nanowire with an average thickness of 112 nm. The rms surface roughness of the etched and oxidized side is smaller than that of the one that was only etched. It is expected that, during thermal oxidation, side line roughness and defects due to anisotropic wet etching were removed. The reduction in surface roughness after thermal oxidation can be explained by the Gibbs-Thompson relationship, which indicates that reactivity depends on the curvature of the rough surface [26]. This is higher at the roughness peaks compared with the roughness troughs. This difference in reaction rates lead to a

smoother surface. Thus, it is advantageous to use the oxidation process during nanowire formation since it results in a smoother surface which consequently reduces surface scattering and improves device performance.

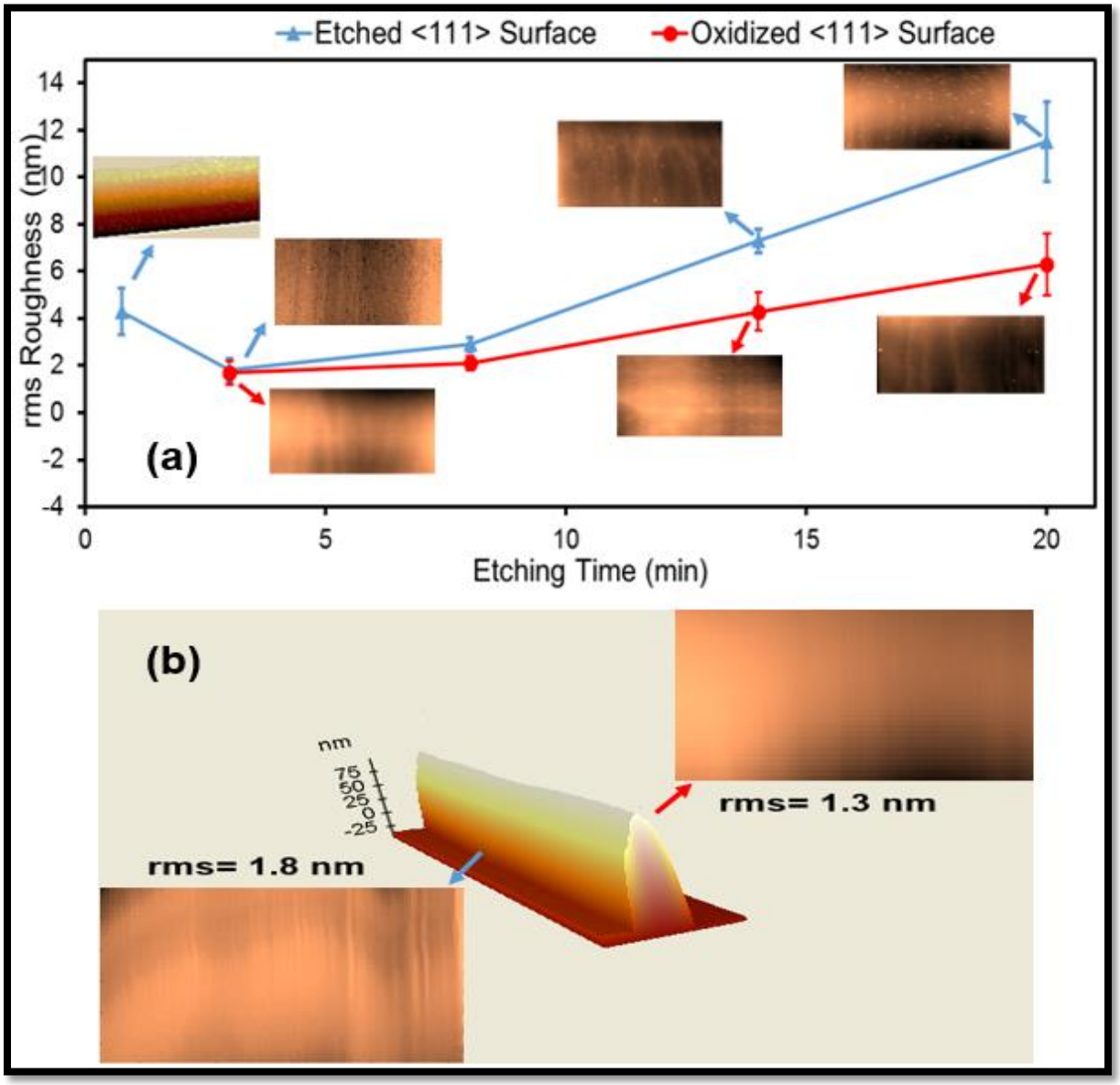

Figure 4. (a) Rms surface roughness of etched <111> surface vs etching time before and after thermal oxidation. The insets show 2D images of the <111> surfaces for different etching times (images length 5 µm), (b) 3D AFM image of nanowire with thickness of 105 nm and length 10 µm. The insets show the 2D image of its surfaces.

3.5. Influence of etchant type on the controllability of the size of the nanowire

In our fabrication process [14], the length of nanowire can be controlled by changing the length of the photomask layer prior to the anisotropic wet etch step. However, the final shape and thickness of the nanowire can be controlled by the conditions under which the first and the second wet etches take place. Thus, a trapezoidal cross-section can be obtained by performing anisotropic etching for a short time during both etch steps; increasing the duration of the second etch results in nanowires with a triangular cross-section. The exact etch time depends on etchant conditions such as chemical concentration and temperature. The thickness of the nanowire can be controlled by the second wet etch time [12].

A high etch concentration with relatively low etch temperature are favoured to obtain better control of nanowire thickness. TMAH and KOH can both be employed to control the size of the nanowire. However, due to its non-zero etching of oxide and slow etch rate, using KOH could cause a failure in the process. Figure 5 shows AFM images of nanowires after placing two samples in KOH at 56 °C for five (left) and eight (right) minutes. The latter shows break occurring along the length of the wire. This indicates that the sidewall oxide was completely etched during the second process. The etch rates of thermal oxide in 40 wt% KOH, 25 wt% TMAH, and 15.6 wt% TMAH at 56 °C were measured as 74 nm/hr, 1.4 nm/hr and 1.6 nm/hr respectively.

It appears that there is no limit to the size reduction of nanowires during etching in TMAH. However, in the case of KOH, the etching of sidewall oxide can limit the ability of the KOH process to obtain a high quality structure at the smallest dimensions. The minimum size of nanowires that can be obtained during KOH etching without any loss or cuts in the nanowires can be given by:

$$y_{min} = t_{si} - (Kt_{tot} - t_c) * \frac{ER_{<111>}}{ER_{SiO_2}} \qquad (7)$$

where t_{si} is the thickness of the silicon layer; t_{tot} is the oxide thickness grown on the sidewall; Kt_{tot} is the oxide thickness remaining on the sidewall after the removal of oxynitride and t_c is the total thickness of oxide consumed during silicon nitride etching, after the removal of oxynitride and the thickness of oxide mask that is required to protect the <111> plane. $ER_{<111>}$ and ER_{SiO_2} are the etch rates of <111> plane silicon and thermally grown silicon dioxide in KOH respectively.

The lateral and vertical reduction of nanowire sizes under different etching conditions are measured for silicon nanowires on bulk silicon wafer (see supplementary information). The relationship between lateral and vertical size reduction is

$$l = 2x = \frac{2y}{\tan\beta} \qquad (8)$$

where l and y are the lateral and vertical size reduction rates respectively and β is the sidewall angle (see supplementary information table S1).

3.5.1 Sub- 10 nm wires

Although our process [14] can be utilized to obtain a well-defined structure with good uniformity; critical dimensions under 20 nm were difficult to obtain when the samples were placed in TMAH for a long time. Moreover, when the etching time is too long, this results in rough nanowires and the variability along the nanowire increases with the increase in etching time. Therefore, to control the etching process in order to obtain sub- 10 nm nanowires, the upper silicon layer of the SOI wafer was chosen to be about 50 nm. Thicker layers can be thinned using thermal oxidation. A 25 wt% TMAH solution added 7.5% IPA at 56 °C was used to reduce the structure, because better controllability can be obtained with a low etch rate solution. As shown in figure 6, 13 nm nanowires were formed after the upper silicon layer of the SOI wafer was reduced to 48 nm using thermal oxidation. The height reduction was measured to be 7 ± 1 nm/min. By controlling experimental conditions, sub-10 nm structures can be repeatedly formed. The smallest dimension of nanowire successfully formed using this method was 6 nm (with an initial silicon thickness of 46 nm and etching time 6 mins) (figure 6(c)). The increase in width of a 6 nm device due to tip geometry, with an AFM tip radius of 10 nm, is calculated to be 12 nm using equation 3.

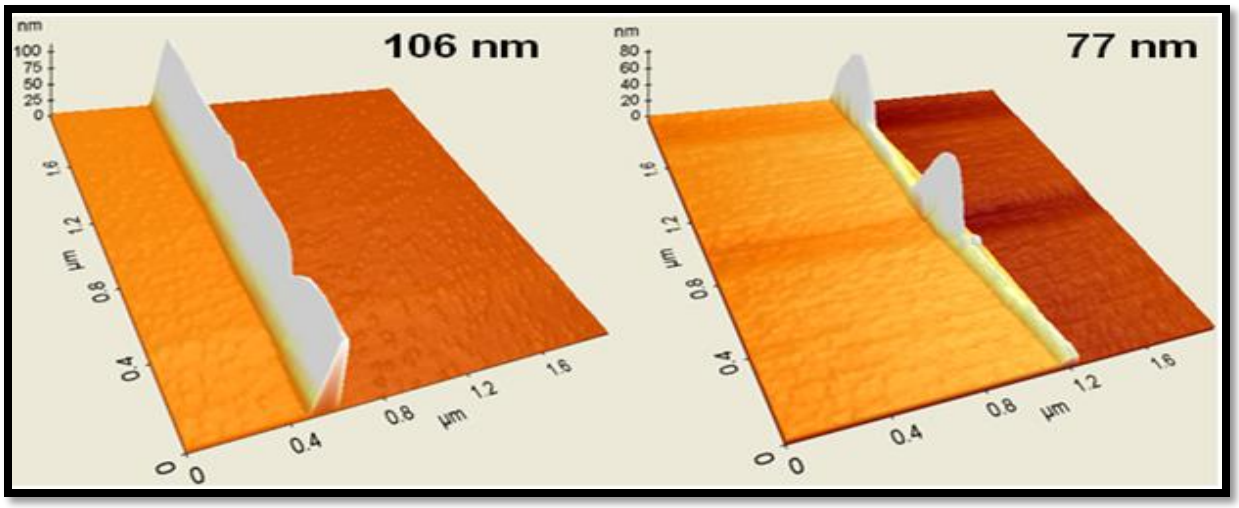

Figure 5. AFM images of nanowires after 5 min (left) and 8 min (right) in 2nd KOH.

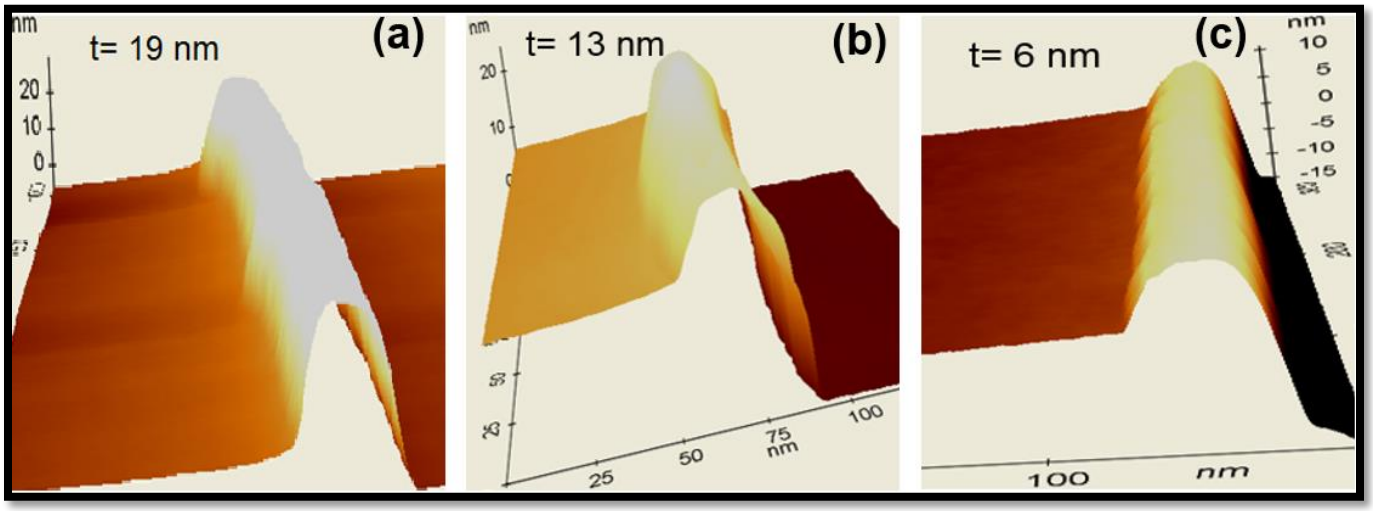

Figure 6. Fabrication of sub 20 nm (a) Nanowire with thickness of 19 nm after 4 mins etching, (b) 13 nm nanowire after 5 mins etching, (c) 6 nm after 6 mins etching.

4. Summary

Sub- 10 nm nanowires were fabricated using simple top-down optical lithography, together with etching and oxidation. We have successfully overcome many issues that otherwise cause fluctuations in nanowire properties. The success of the fabrication process strongly depends on the robustness of silicon nitride during thermal oxidation. Nitrogen-rich silicon nitride films are preferable as an oxidation mask since they exhibit the lowest oxidation rate and the highest etch rate in boiling phosphoric acid in comparison with silicon-rich silicon nitride films. The size and the shape of the nanowires were controlled using oxidation and anisotropic etching. Using this method, nanowires with different thicknesses from 6 nm to 100 nm were fabricated.

AFM scans revealed rms surface roughness after image processing. Thermal oxidation was shown to improve the surface roughness which could be important in optimizing device performance when integrating nanowires into

functional devices. These devices have the potential to be integrated with CMOS into intelligent functional systems that can exploit their nanoscale dimensions, such as biosensing or energy harvesting.

References

[1] Y. Cui, Q. Wei, H. Park, and C. M. Lieber, "Nanowire nanosensors for highly sensitive and selective detection of biological and chemical species," *Science,* vol. 293, pp. 1289-1292, 2001.

[2] A. I. Boukai, Y. Bunimovich, J. Tahir-Kheli, J. K. Yu, W. A. Goddard Iii, and J. R. Heath, "Silicon nanowires as efficient thermoelectric materials," *Nature,* vol. 451, pp. 168-171, 2008.

[3] A. I. Hochbaum, R. Chen, R. D. Delgado, W. Liang, E. C. Garnett, M. Najarian, *et al.*, "Enhanced thermoelectric performance of rough silicon nanowires," *Nature,* vol. 451, pp. 163-167, 2008.

[4] E. Garnett and P. Yang, "Light trapping in silicon nanowire solar cells," *Nano Letters,* vol. 10, pp. 1082-1087, 2010.

[5] L. Tsakalakos, J. Balch, J. Fronheiser, B. A. Korevaar, O. Sulima, and J. Rand, "Silicon nanowire solar cells," *Applied Physics Letters,* vol. 91, 2007.

[6] K. I. Chen, B. R. Li, and Y. T. Chen, "Silicon nanowire field-effect transistor-based biosensors for biomedical diagnosis and cellular recording investigation," *Nano Today,* vol. 6, pp. 131-154, 2011.

[7] J. T. Robinson, M. Jorgolli, A. K. Shalek, M. H. Yoon, R. S. Gertner, and H. Park, "Vertical nanowire electrode arrays as a scalable platform for intracellular interfacing to neuronal circuits," *Nature Nanotechnology,* vol. 7, pp. 180-184, 2012.

[8] B. Tian, T. Cohen-Karni, Q. Qing, X. Duan, P. Xie, and C. M. Lieber, "Three-dimensional, flexible nanoscale field-effect transistors as localized bioprobes," *Science,* vol. 329, pp. 830-834, 2010.

[9] K. Trivedi, H. Yuk, H. C. Floresca, M. J. Kim, and W. Hu, "Quantum confinement induced performance enhancement in sub-5-nm lithographic Si nanowire transistors," *Nano Letters,* vol. 11, pp. 1412-1417, 2011.

[10] C. Wang, M. E. Jones, and Z. A. K. Durrani, "Single-electron and quantum confinement limits in length-scaled silicon nanowires," *Nanotechnology,* vol. 26, 2015.

[11] K. S. Yi, K. Trivedi, H. C. Floresca, H. Yuk, W. Hu, and M. J. Kim, "Room-temperature quantum confinement effects in transport properties of ultrathin si nanowire field-effect transistors," *Nano Letters,* vol. 11, pp. 5465-5470, 2011.

[12] S. Chen, J. G. Bomer, W. G. Van der Wiel, E. T. Carlen, and A. Van Den Berg, "Top-down fabrication of sub-30 nm monocrystalline silicon nanowires using conventional microfabrication," *ACS Nano,* vol. 3, pp. 3485-3492, 2009.

[13] K. Itoh, K. Iwameji, and Y. Sasaki, "Fabricating of thin silicon wires by anisotropic wet etching of SOI structures," *Japanese Journal of Applied Physics, Part 2: Letters,* vol. 30, pp. L 1605-L 16, 1991.

[14] N. F. Za'Bah, K. S. K. Kwa, L. Bowen, B. Mendis, and A. O'Neill, "Top-down fabrication of single crystal silicon nanowire using optical lithography," *Journal of Applied Physics,* vol. 112, 2012.

[15] H. Du, R. E. Tressler, K. E. Spear, and C. G. Pantano, "Oxidation studies of crystalline CVD silicon nitride," *Journal of the Electrochemical Society,* vol. 136, pp. 1527-1536, 1989.

[16] M. A. Pereira, J. A. Diniz, I. Doi, and J. W. Swart, "Silicon nitride deposited by ECR-CVD at room temperature for LOCOS isolation technology," *Applied Surface Science,* vol. 212-213, pp. 388-392, 2003.

[17] S. Callard, A. Gagnaire, and J. Joseph, "Fabrication and characterization of graded refractive index silicon oxynitride thin films," *Journal of Vacuum Science and Technology A: Vacuum, Surfaces and Films,* vol. 15, pp. 2088-2094, 1997.

[18] P. G. Snyder, Y. M. Xiong, J. A. Woollam, G. A. Al-Jumaily, and F. J. Gagliardi, "Graded refractive index silicon oxynitride thin film characterized by spectroscopic ellipsometry," *Journal of Vacuum Science and Technology A,* vol. 10, pp. 1462-1466, 1992.
[19] H. G. Tompkins and E. A. Irene, *Handbook of Ellipsometry*, 2005.
[20] *Winelli II Tutorial Manual* 1.1.0.67 ed., 2004.
[21] M. Fouchier, E. Pargon, and B. Bardet, "An atomic force microscopy-based method for line edge roughness measurement," *Journal of Applied Physics,* vol. 113, 2013.
[22] V. Senez, D. Collard, P. Ferreira, and B. Baccus, "Two-dimensional simulation of local oxidation of silicon: Calibrated viscoelastic flow analysis," *IEEE Transactions on Electron Devices,* vol. 43, pp. 720-731, 1996.
[23] V. K. Dwivedi, "Bird's-beak-free sealed-interface local oxidation technology for submicron ultra-large-scale integrated circuits," *Journal of the Electrochemical Society,* vol. 137, pp. 2586-2588, 1990.
[24] M. Yun, "Investigation of KOH anisotropic etching for the fabrication of sharp tips in Silicon-on-Insulator (SOI) material," *Journal of the Korean Physical Society,* vol. 37, pp. 605-610, 2000.
[25] W. Haiss, P. Raisch, L. Bitsch, R. J. Nichols, X. Xia, J. J. Kelly, *et al.*, "Surface termination and hydrogen bubble adhesion on Si(1 0 0) surfaces during anisotropic dissolution in aqueous KOH," *Journal of Electroanalytical Chemistry,* vol. 597, pp. 1-12, 2006.
[26] D. K. Sparacin, S. J. Spector, and L. C. Kimerling, "Silicon waveguide sidewall smoothing by wet chemical oxidation," *Journal of Lightwave Technology,* vol. 23, pp. 2455-2461, 2005.