Reducing Switching Noise Effects by Advanced Clock Management

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***Abstract*—In this paper an overview of different clock management methods for the reduction of switching noise is provided. On one hand, standard design-flow compliant methods such as current shaping and clock modulation can be successfully applied, especially for targeting higher harmonics of the switching noise. On the other hand, methods deploying globally-asynchronous locally-synchronous (GALS) circuits can result in very effective noise reduction of lower harmonics. With this approach it can be shown that, when a power-balanced GALS partitioning scheme is used, the switching noise reduction at lower harmonics of the clock frequency corresponds to 20logM, where M is the number of GALS partitions. A complex gigabit OFDM DSP processor, named the Moonrake chip demonstrates switching noise reduction of over 20 dB using a pausible clocking GALS architecture. The Lighthouse chip, integrating a mixed-signal 120 GHz Radar transceiver, demonstrates the potential for reducing the substrate noise. Finally, the Screamer chip, performing the function of a trusted sensor node, shows that current shaping techniques based on synchronous circuits can be successfully utilized for switching noise reduction, achieving more than 10 dB improvement in the target frequency range.**

Keywords—switching noise, substrate noise, GALS, current shaping

I. INTRODUCTION

Synchronous clock activity in digital circuits represents a very significant noise source which can manifest itself in different ways. The increase of dynamic IR drop and ground bounce is possible due to clock activity, leading to performance reduction or even malfunction of the digital block itself. Moreover, the negative impact of the switching noise is not limited to the digital circuit part only. In mixed-signal circuits it can propagate over the substrate influencing the neighboring analog circuitry. Finally, such noise propagation is possible also outside the chip causing EMI (electromagnetic interference).

There are several methods to address the negative effects of switching noise. The usual approach includes integration of a large number of decoupling capacitors placed in- and outside the chip [1]. This method is effective; however, it comes also with the price of increased chip area and power consumption. Therefore, alternative approaches are used, such as current shaping of the clock – i.e. to introduce variations of phases in the synchronous clock activity. In this way, the flip-flops driven by the clock signal are separated into different groups, each with some defined phase difference with respect to the original clock [2]. In this way, the steep current peaks are avoided, leading to the noise reduction, mainly in the time domain. Additionally, it is possible to modulate the clock source by applying some jitter to the clock. This approach will reduce the noise in the spectral domain, especially for the higher harmonics [2, 3].

In this work, we will give an overview of methods for clock management which can be applied for switching noise reduction, as demonstrated by the test circuits described in the text. This includes techniques based on synchronous circuits as well as the utilization of globally asynchronous locally synchronous (GALS) design techniques, where the digital block is partitioned into different internally synchronous blocks which communicate in an asynchronous fashion [4].

In the next section the main methods for switching noise reduction in the spectral domain will be introduced. Thereafter, a theoretical overview will be provided. This is followed by the results of silicon validations in test chips in different technologies and for different applications.

II. ADVANCED METHODS FOR SWITCHING NOISE REDUCTION

In the following section, we will briefly describe some of the main techniques which can be applied for clock management with the aim of reducing the switching noise in the frequency domain.

A. Synchronous Current Shaping

One of the most effective methods to decrease the switching noise in the time domain is current shaping or clock scheduling. The basic idea of this approach is to partition the standard synchronous design into subdomains. The clock trees for such subdomains are consequently planned to introduce the specific phase difference between domains which should make the overall current shape much smoother. This method is very efficient in reducing IR drop, ground bounce and other effects

related to the switching noise in time domain. However, it is possible to address the noise in the frequency domain, especially in the higher harmonics, as will be analyzed in the next section. The major implementation challenges in this methodology are related to the setup/hold timing closure after phase shift insertion [11].

B. Clock Modulation

One alternative methodology is called clock modulation or spread spectrum clocking (SSC). This method is based on intentional insertion of jitter to the clock source. This method is fully focused on switching noise reduction in the frequency domain and more effective at higher harmonics [7]. The detailed analysis is provided in the next section. Clock modulation can be fairly simple implemented, either off-chip or on-chip, using programmable delay lines. This method additionally increases the critical path in the system by the maximal phase difference between two clock cycles reducing the maximal design performances.

C. Power-balanced plesionchronous GALS methodology

More aggressive clocking schemes can be applied if the partitioned synchronous domains are interfaced using asynchronous handshake wrappers, generating GALS system. In this work the focus is on the GALS method based on a pausible clocking architecture [4, 5, 6, 7, 8], where each locally synchronous block is driven by an independent ring-oscillator-based clock generator. Nevertheless GALS methodology can be successfully applied for noise reduction using more "designer friendly" methods, for example based on asynchronous FIFOs for interfacing. GALS systems can be implemented using different clocking scenarios, from mesochronous, where all local clocks are using the same frequency but with undefined phase shift, to plesiochronous, where the blocks use almost the same frequency, up to the fully asynchronous, where GALS blocks use completely different clock frequencies. In this work the major focus is on pleasiochronous clocking, which enables effective noise reduction, but still not differing significantly from the usual synchronous approach. The proposed partitioning methodology for such a clocking scheme is based on power-balancing where the GALS blocks have approximately equal power consumption. This method can be effectively used for the switching noise reduction in the frequency domain as elaborated in the next section. The major implementation challenges of such an approach are coming with the necessity for insertion of asynchronous interfaces which can bring additional performance losses and area/power increase. Moreover, the control flow in GALS systems is more complex since it cannot rely on the data availability in particular local clock cycle but it must work in the data-flow way.

III. Modeling of the Switching Noise Reduction in Frequency Domain

A. Switching Current Model

It has been shown [2][9] that the switching current spectrum in digital integrated circuits can be separated in two components: discrete peaks and continuous noise floor. Discrete peaks correspond to clock period averaged switching current waveform, while the noise floor corresponds to the fluctuations in waveforms between the clock periods. The peaks are remarkably above the noise floor, and most power is concentrated in them.

In order to be able to analyze the effectiveness of methods for switching current reduction on higher level of abstraction, a simplified representation of the switching current waveform has to be introduced. It has been shown that for medium-scale digital systems (about 40 thousand gates in 2005 [2]) the clock period averaged current waveform can be represented as a periodic triangular signal. Such model is shown in Fig. 1.

The magnitude of the n^{th} harmonic in the spectrum of such signal is [5]:

$$\left|F_n\right| = \frac{I_p}{2\pi n}\left|\operatorname{sinc}(\pi n f_0 t_r) - \operatorname{sinc}(\pi n f_0 t_f)\, e^{-j\pi n f_0 (t_r + t_f)}\right| \qquad (1)$$

B. Synchronous Current Shaping

In case of synchronous current shaping (SCS) by clock skew insertion [2], the noise reduction is achieved by spreading the time domain waveform. There is still just one single clock in the system, but the purposely introduced skew spreads the switching activity in time domain. In the simplified triangular mode, this can be seen as extending the relative width of the triangle, while maintaining its area (because the average charge which is consumed in each clock cycle remains approximately the same).

For high harmonics, satisfying the following condition [5]:

$$nf_0 > \max\{\frac{1}{\pi t_r}, \frac{1}{\pi t_f}\} \qquad (2)$$

the magnitude of the nth harmonic in the switching current spectrum can be expressed as:

$$a(nf_0) \geq \frac{4Qf_0}{(\pi n\lambda)^2} \qquad (3)$$

where λ is the relative width of the triangular pulse:

$$\lambda = (t_r + t_f)\, f_0 \qquad (4)$$

The factor λ shows the dependence of magnitude on the current shaping. The magnitude reaches its minimum for $\lambda = 1$.

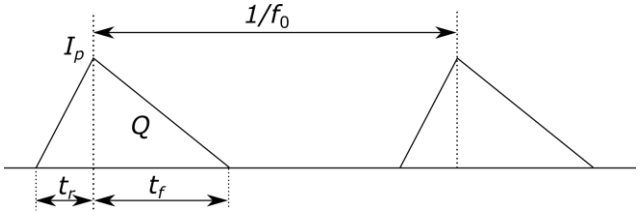

Figure 1: Triangular model of digital switching current.

In that case, the maximum attenuation achieved is:

$$A_{dB}(nf_0) \approx 40\log(1/\lambda_0) \quad (5)$$

where λ_0 is the relative width of the triangular pulse for the initial system, before current shaping.

For low harmonics, however, it can be shown [5] that the magnitude is:

$$a(nf_0) \approx Qf_0 \quad (6)$$

which means that it's not dependent on the current shaping at all.

Thus, with λ increasing, the noise magnitude for high harmonics decreases with a rate $1/\lambda^2$, while the change in noise magnitude at low harmonics is only marginal. Additionally, the maximum clock skew, i.e. the maximum λ stretching, is limited due to timing constraints imposed by the RTL design, which also limits the efficiency of this method.

C. Clock Modulation (Spread Spectrum Clocking)

In case of spread spectrum clocking (SSC) [2], the clock frequency is being modulated by a frequency modulation. As a result, the power of each spectral peak is spread over a wider bandwidth, resulting in harmonic peak attenuation. According to the Carson's law, the noise peak reduction at n^{th} harmonic can be expressed as [12]:

$$A_{dB}(nf_0) \approx 10\log(2(n\beta+1)) \quad (7)$$

where β is the modulation index of the frequency modulation of the clock, defined as a ratio:

$$\beta = \Delta f / f_m \quad (8)$$

where Δf is the peak frequency deviation from the central frequency, and f_m is the clock modulation frequency. For low harmonics, below the limit:

$$n_{cutoff} = 1/\beta \quad (9)$$

the attenuation is only marginal. On the other hand, at higher frequencies, an overlapping of bands corresponding to adjacent harmonics can occur, which reduces the achievable attenuation. The limit at which this starts to happen can be expressed as [10]:

$$n_{overlap} = \frac{1}{\beta}\left(\frac{f_0}{2f_m} - 1\right) - \frac{1}{2} \quad (10)$$

For the harmonics between these two limits, a significant attenuation can be achieved. The attenuation can be further improved by increasing β. However, this comes at a cost of lowering the $n_{overlap}$ limit. Another issue is that the achievable β is limited by the achievable Δf – increasing Δf also lowers the average throughput.

D. Power-Balanced Plesionchronous GALS Methodology

In plesiochronous GALS designs, an originally synchronous system is divided into several clock domains, called the locally synchronous modules (LSMs). Each of the LSMs has its own clock, but the frequencies of these local clocks have only a slight mismatch from the central frequency, i.e. from the original synchronous clock. Because of that, each harmonic peak from the synchronous system is replaced by M smaller spectral peaks, where M is the number of LSMs.

Using the triangular switching current model, the peak attenuation achieved this way at lower harmonics can be expressed as [8]:

$$A_{dB}(nf_0) \approx 20\log\frac{\sum_{m=1}^{M}\overline{P_m}e^{-j\pi n\lambda_m}}{\max(\overline{P_m})} \quad (11)$$

where $\overline{P_m}$ is the average power dissipation of m^{th} clock domain, and λ_m is a factor related to the relative width of the triangular current pulse:

$$\lambda_m = (t_{rm} + (t_{rm} + t_{fm})/2)\, f_m \quad (12)$$

The optimum attenuation is achieved if the LSMs are balanced in terms of power [8]:

$$\overline{P_m} = P_{total}/M, \quad 1 \le \forall m \le M \quad (13)$$

and it can be expressed as:

$$A_{dB}(nf_0) \approx 20\log M + O(\Lambda) \quad (14)$$

where $O(\Lambda)$ is an offset term, showing dependence of the attenuation on the relative widths of triangular pulses. For large M, this influence is negligible, and the attenuation can finally be expressed as [8]:

$$A_{dB}(nf_0) \approx 20\log M \quad (15)$$

E. Comparison of Methods for Switching Noise Reduction

Table I. summarizes the properties of the three switching noise reduction methods.

TABLE I. PROPERTIES OF THE ADVANCED SWITCHING NOISE REDUCTION METHODS

Method	**Maximum attenuation**	
	Low harmonics	***High harmonics***
SCS	**marginal, if any at all**	**$40\log(1/\lambda_0)$**
SSC	**$10\log(2(n\beta+1))$ low due to low $n\beta$**	**$10\log(2(n\beta+1))$, $n<n_{overlap}$**
P-bal. plesio. GALS	**$20\log M$**	**not targeted**

SCS can achieve a remarkable attenuation at higher harmonics. However, since this attenuation depends on the waveform factor λ, it relies on the estimation of the current shape, which is not available for mainstream CAD tools. At low harmonics, the attenuation achieved with this method is negligible. SSC achieves good attenuation for the harmonics between the two limits, n_{cutoff} and $n_{overlap}$. The attenuation gets

better for higher harmonics, until the $n_{overlap}$ limit is reached, and for harmonics above that limit it drops significantly due to spectrum overlapping. For low harmonics, high attenuation could be achieved only by setting a large value of the modulation index β, which is usually not achievable in practice. Increasing β lowers the throughput, and also degrades the attenuation at higher harmonics due to lowering the $n_{overlap}$ limit. In general, both SCS and SSC provide just a limited performance, if any, regarding noise attenuation at the clock frequency and low harmonics. It has to be stressed that the noise power of switching current is dominated exactly by the fundamental and low harmonics, which makes them the most important attenuation targets.

Power-balanced plesiochronous GALS design, on the other side, targets exactly those spectral components. It can provide a noise peak drop of 20log(M) for M LSMs, which outperforms the other two methodologies. Besides, unlike SCS, this methodology is not dependent on current shape estimation, but solely on power estimation, which can be easily obtained in mainstream CAD tools, and on the number of LSMs. This makes the power-balanced plesiochronous GALS design a robust and predictive methodology.

IV. Silicon Demonstrators and Results

In the following section the theoretical results have been further evaluated in silicon on the number of test ASICs.

A. *Moonrake Chip (2010, 40 nm CMOS)*

Moonrake chip represents the silicon validation of the pausible clocking GALS scheme for switching noise reduction in the frequency domain. This chip has integrated full OFDM baseband transmitter DSP, implemented in two fashions: as baseline synchronous circuit and as GALS implementation. The implemented circuit is relatively complex with estimated gate count of 7.8 Million gates. In the GALS version the proposed pausible clocking scheme has been used, and the complete transmitter design has been partitioned in 6 plesiochronous GALS domains. Power- and area-balanced partitioning has been used to establish the different GALS domains. This chip has been designed and manufactured in 40 nm CMOS process. The layout photo of Moonrake chip is provided in Figure 2.

The measurements have been focused on the power/area evaluation as well as the evaluation of the spectral amplitude of the core Vdd which should indicate the switching noise effects. The summary of the measurement evaluation has been provided in Table II. GALS version has under same performance setting utilized the smaller power consumption of about 8.2%. This improvement is mainly due to the reduced complexity of the local clock trees of GALS design compared to the complex global clock tree of the synchronous design. It is estimated that the clock network has been reduced 3.6 times due to this approach. Such reduction has also affected the area utilization which was also improved for GALS design due to the simpler clock network and replaced PLL with the small local pausible clock oscillators. Finally, the measurement of the spectral amplitude of the core supply has revealed the dramatic difference in the switching noise, which was up to 26 dB of the first harmonic, 16 dB of the second and 30 dB of the third harmonic. The measurement results are beyond the expected reduction, which is probably due to the additional effect of clock tree reduction, which is not part of the model, but also due to the vicinity of the test pin to the synchronous block. The additional measurements performed on the supply lines on the board have shown the reduction of the first harmonic of 19 dB.

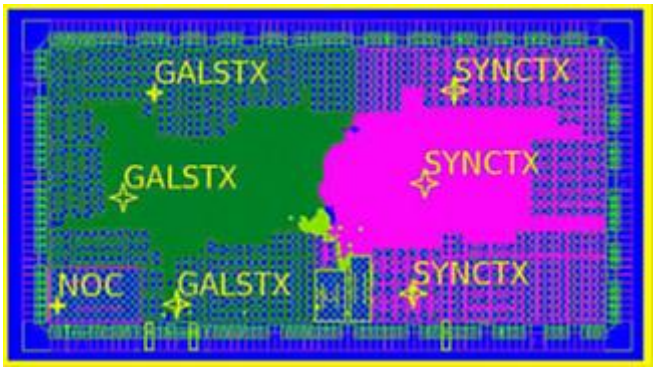

Figure 2: Layout photo of Moonrake Chip [6]

TABLE II. Summary of the Moonrake Chip evaluation

	Area (mm^2)	Power (mW)	Spectral amplitude of Core VDD (dBm)		
			1st peak	2nd peak	3rd peak
Sync. Tx	2.33	258	-15	-32	-23
GALS Tx	2.22	237	-41	-48	-53
Diff.	**+4.7%**	**+8.2%**	**26dB**	**16dB**	**30dB**

B. *Lighthouse Chip (2012, 130 nm BiCMOS)*

Lighthouse chip has been focused on evaluation of the effects and potential reduction of the switching noise in the mixed-signal circuits. In particular, this design includes the implementation of FMCW radar in 120 GHz band fabricated in 130 nm BiCMOS technologies. The two variants, synchronous and pausible clocking GALS of the baseband processor have been implemented in this chip for fair comparison. The baseband processor contains as a major processing block 4096-point FFT which has been partitioned in five different plesiochronous domains using power-balanced partitioning method. The die photo is given in Figure 3.

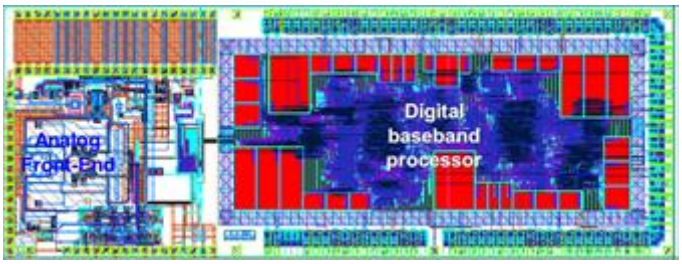

Figure 3: Die photo of the Lighthouse chip [8]

The measurement of the voltage variation spectrum at the supply pad has shown a reduction of 12.29 dB for the fundamental frequency. This corresponds to the value expected from the theoretical model. The measurement pin has been exactly placed between the GALS and synchronous core enabling fair comparison. Due to the relatively low-complexity of this design, GALSification lead to some increase in the silicon area and in power consumption which is 4.3% and 6.6%, respectively.

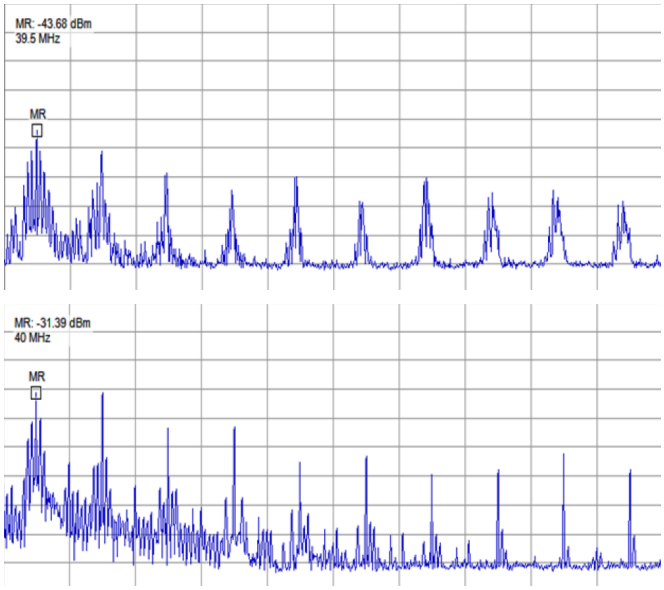

Figure 4: Spectrum of the power supply when baseband processor operates in GALS (upper) and synchronous (lower) mode [8]

C. Screamer Chip (2014, 130 nm BiCMOS)

The SCREAMER chip has been evaluating the synchronous methods using a SCS based methodology for switching noise reduction in the frequency domain. The target circuit has been a Trusted Sensor Node (TSN) design, containing several cryptoprocessing blocks (AES, ECC, SHA-1 co-processors) as well as a LEON-2 processor. This design has been implemented using different optimization methods in four different ways: one baseline design (no current shaping), two different optimization using the FloorDirector CAD tool from company Teklatech, and finally one pre-conditioned design where on top of FloorDirector optimization the system has been split into two clock domains, each working with different clock edge of the main clock. The layout photo of this design has been shown in Fig. 5.

While the basic approach is SCS, rather than simply spreading the clock, the optimization has specifically been targeting the improvements in the frequency domain, and moreover a particular frequency range, as supported by FloorDirector. Therefore, the optimization had to take into account also the actual test scenario activity, as well as the dynamic power waveforms, in order to optimize the switching activity correspondingly. The selected target band was around 850 MHz, which is a corresponding to ISM band frequently used for wireless sensor node communication. The design flow of the different macros was essentially the same (apart from design changes for two-phase clocking in macro 3) until the phase of the CTS (clock tree synthesis). At this stage the FloorDirector has been analyzing design and proposing optimized clock scheduling in order to reach maximal switching noise reduction in the target band. After CTS, the remaining steps have been again in all cases corresponding to the usual design flow.

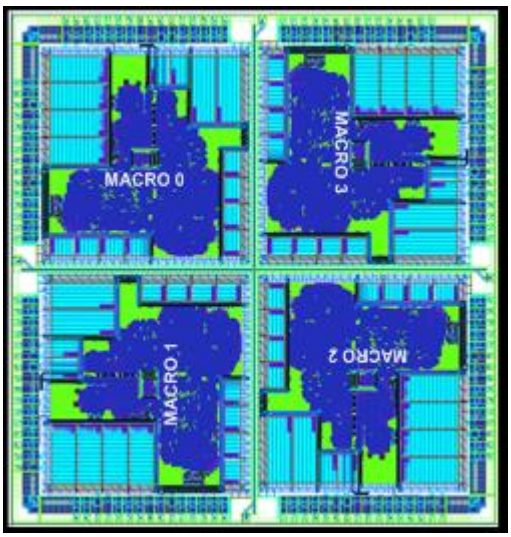

Fig 5: Layout photo of SCREAMER design with 4 different TSN macros [5]

The measurement strategy has been focused on evaluating substrate noise, as measured on a substrate contact placed in the middle of each macro. The significant reduction of the substrate noise has been found. The comparison of all four macros, with the focus on target band has been provided in Fig. 6.

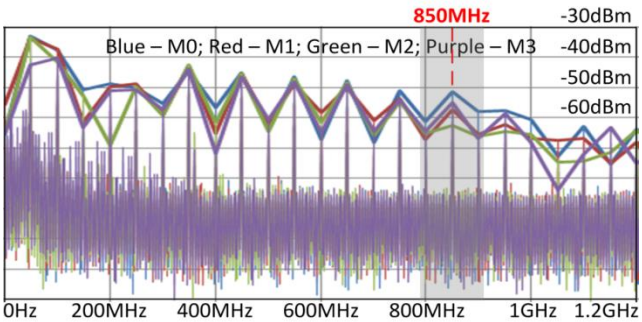

Fig. 6: Substrate noise at the different frequency harmonics for all 4 TSN macros [5]

In the target band the achieved substrate noise reduction was maximal for macro 2, and corresponding to 11.1 dB. As shown in Fig 6, the targeted band around 850 MHz is visibly reduced over other bands, indicating how the specific focus on frequency domain optimization is realized. It is worth to mention that the 2-phase clocking was quite effective for reduction of the first harmonic of EMI, achieving 9.6 dB. The

spectral peaks measurements of substrate noise have been summarized in Table III.

TABLE III. SPECTRAL PEAKS AT THE DIFFERENT HARMONICS IN DB

	Macro0	Macro1	Macro2	Macro3
50 MHz	-32.8	-33.5	-33.3	-42.4
800 MHz	-63.1	-67.1	-65.2	-64.5
850 MHz	-51.3	-57.2	-62.4	-55.0
900 MHz	-58.1	-65.3	-66.1	-66.7

V. SUMMARY AND CONCLUSIONS

In this paper, an overview of different methods for switching noise reduction is provided. It has been demonstrated that methodologies based on clock activity management can efficiently reduce the generation of switching noise both, in time domain and in the frequency domain.

Among the available methods, in this work we have mainly focused on clock scheduling and GALS clock management, which allows fully staying in the synchronous domain of operation. The methods have been theoretically modelled and evaluated, showing the pros and cons for the different methodologies.

The noise reduction expected from the theoretical model provided in Section III have been confirmed in a number of silicon demonstrators, including the chips Moonrake, Lighthouse and Screamer. It has been confirmed that in the case of GALS technique with plesiochronous clocking the excellent switching noise reduction can be obtained at the frequency of the first harmonic of the clock. This reduction is comparable to theoretically expected 20 Log N, where N is the number of partitions. On the other hand, it has been additionally shown that the standard-flow compliant SCS-based methods can be successfully applied for the reduction of the targeted higher harmonic of the switching noise. In the produced SCREAMER chip this benefit was almost 10 dB in the target frequency bend.

This analysis reflect the effect of different clocking strategies with various degree of modification of the standard design flow, and so in the future, we plan to explore deeper the EDA aspects for EMI, as well as power supply modulation as in many mixed-signal applications the future design will involve both data processing and power management electronics.

ACKNOWLEDGMENT

This work has been supported by the European Project GALAXY under grant reference number FP7-ICT-214364, European Project SUCCESS under grant reference number FP7-ICT-248120, and EU Eurostars program under the Grant No. E7531.

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