Online Condition Monitoring of Sub-module Capacitors in MMC Enabled by Reduced Switching Frequency Sorting Scheme

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***Abstract*—This paper presents a novel condition monitoring scheme for sub-module (SM) capacitors in the modular multilevel converter (MMC), where the fast-affine projection (FAP) algorithm is cooperatively embedded in a dedicated range-based sorting scheme with reduced switching frequency to estimate the capacitor parameters. The proposed sorting scheme not only reduces the switching events of SMs, but also manages to maintain the capacitor ripple voltage within an acceptable range. Whilst the use of FAP achieves an on-line parametric estimation with superior speed and accuracy. Compared to previous studies, this proposed approach has significant advantages in terms of estimation accuracy and speed without the need for extra hardware. The effectiveness of the proposed approach is validated by a 5-level MMC model in MATLAB/Simulink. From simulation results, the estimation speed is less than 1.5 ms and the error is less than 3%.**

Keywords—condition monitor; modular multilevel converters; reduced frequency sorting scheme; fast affine projection

I. INTRODUCTION

The modular multilevel converter (MMC) was first introduced in 2001[1] and developed rapidly in recent years. This topology is suitable for medium to high power applications especially for the high-voltage direct current (HVDC) transmission due to its high-quality output voltage. It exhibits enormous advantages over other conventional converters including modularity and scalability, lower switching frequency, less requirement for ac filters, the absence of dc-link capacitors and inherent redundancy for sub-module (SM) failure management[3]

The capacitors are the weakest components in power converters[4] compared with diodes, semiconductors and other switches. According to Fig.1, nearly 30% failure of power electronic devices is capacitors. However, few of researches have focused on such area because of its nature of passive components, but it does play an important role in many areas, especially for MMC, where hundreds of SMs are there in the real projects. Due to the series connection, any failure of the signal could lead to severe problems.

In order to maintain reliable operation of power electronic system, a suitable capacitor monitoring method is required to ensure every capacitor are under their appropriate condition.

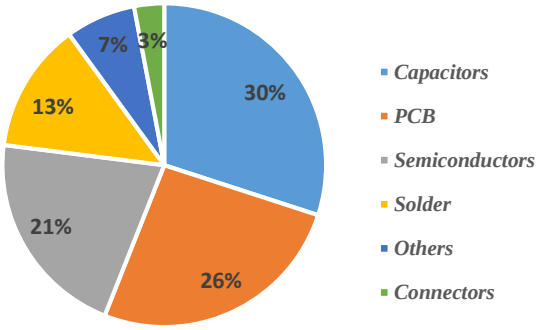

Figure 1. The failure rate of power electronic devices [2]

Based on criteria handbook[5], the aluminium capacitor can be defined as 'failure' when it lost 20% capacitance or its equivalent series resistance (ESR) increased 50%. Meanwhile, for film capacitors, the failure criteria is even more strict, where the failure is been defined when its capacitance has a 5% reduction or its dissipation factor increase 3 times ($\tan\delta = \omega RC = R/X_C$)[6]. Therefore, the condition monitoring methods of the capacitor must have good accuracy to detect the parameters' variation.

The complexity of MMC circuits demands a huge number of sensors implement the condition monitor, which increase the cost and reduce the reliability. Therefore, the estimation of capacitance and its ESR as health indicators is the most suitable method in such complicated converter topologies[2]. By comparing the estimated variables with the pre-defined failure criteria, the condition of capacitors can be evaluated. The conventional way is to measure the voltage and current ripple directly, then calculate the capacitance and ESR depending on the dominant frequency region of impedance[7], but requires additional filters. The [8] tries to extract 2nd order harmonic of ripple voltage and current and extract them by a band-pass filter (BPF) to estimate the capacitance, this offline method is suitable for dc-dc converters but performs badly in terms of error on MMC topologies. In recent years, the software-based algorithms draw more attention, in[9], for a dc-link capacitor, an AC

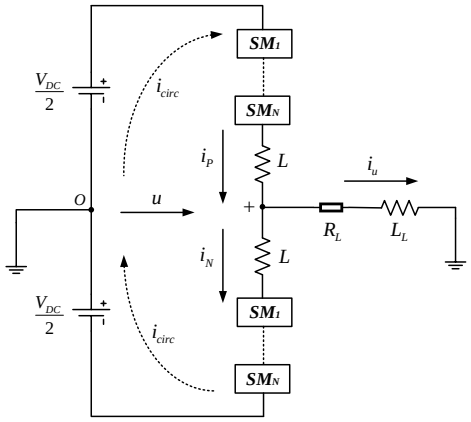

Figure 2. Single-phase MMC configuration

signal was injected to the reference PWM and a digital band-pass filter is used for signal extraction, then the capacitance is calculated using recursive least square (RLS) algorithm. An RLS-based method is applied for MMC sub-modules in[10], which requires extra signal injection and filters but the speed is relatively fast. The Kalman-filter is introduced for SM voltage estimation is described in[11], this method needs to estimate the voltage first before estimate the capacitor so the speed is slow. References [12] present techniques to estimate capacitor voltages by predictive algorithms which provide another way to monitor the capacitors by virtual signals, however, the effectiveness of monitoring the capacitor needs to be further validated.

This paper proposes a condition monitoring approach for SM capacitors in MMC. It consists of a switching reduction sorting scheme and a designated estimation algorithm. The collaboration of the dedicated sorting scheme and estimation algorithm achieves a fast and accurate estimation of capacitor parameters without interrupting the system operation. It requires no extra hardware and is applicable to both online and offline applications. Section II describes the MMC operation and conventional voltage balancing strategy associated with the capacitor issues. Section III depicts the proposed range-based sorting scheme and the collaboration with the FAP algorithm. Section IV reports the simulation validations from a 5-level MMC inverter. The results are comprehensively compared with the previous studies and the conclusion is presented in Section V.

II. THE OPERATION OF MMC

Fig.2 shows a typical one leg of three-phase MMC topology, which consists of two arms, and each contains *N* sub-modules and one inductor. The circulating current within each leg of the MMC has a significant impact on the ratings of the power devices, capacitor voltage ripple and power losses[13].

The SM has four operation models based on the switching statues and the arm current direction. It worth noting that the two complimentary power switches in each SM have opposite driving signals, as shown in Table I. If the upper switch **S1** is switched on while lower switch **S2** is switched off, the arm

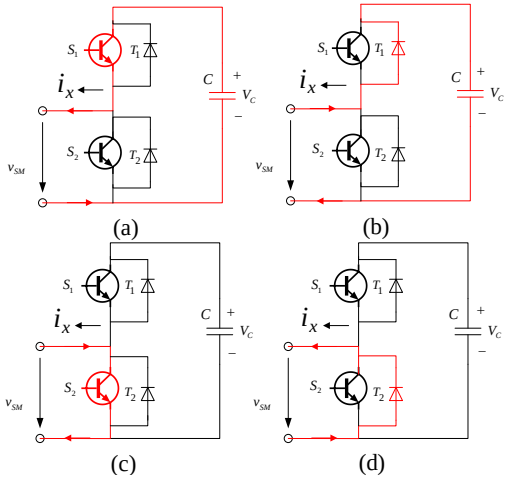

Figure 3. Operational switching states of SM

TABLE I. Basic operation modes of SM

T1	T2	Vo	Current Direction	Capacitor State
ON	OFF	v_c	$i_x > 0$	Charging
ON	OFF	v_c	$i_x < 0$	Discharging
OFF	ON	0	$i_x > 0$	Bypassed
OFF	ON	0	$i_x < 0$	Bypassed
OFF	OFF	0	N/A	N/A

current flow through the capacitor, so the SM voltage V_0 is equal to capacitor voltage V_C. The state of the SM is defined as ON-STATE, the capacitor voltage is connected with other ON-STATE capacitors and contributes to the output voltage levels of MMC. Meanwhile, if the upper switch **S1** is switched off and the lower switch **S2** is switched on, the arm current does not flow through the capacitor, the SM capacitor is get bypassed which means the capacitor is isolated from the main circuit, so the SM voltage $V_0 = 0$. The state of the SM is defined as OFF-STATE. The operation model and the current path are illustrated in Fig.3 for clarity. In addition, there are fault switching states when both two switches are switched off.

In order to balance the voltage of sub-modules at reference value with acceptable oscillations. A larger number of papers has proposed relative methods to solve it. Among them, the sorting algorithm is the most popular method [14]. The method is straightforward compared with others: Select the SMs with the lowest voltages to open and the SMs with the highest voltages to close. After detecting the direction of the arm current, the algorithm will identify the system state. If the current in upper or lower arm is positive, then the algorithm will find the SM with the lowest voltage and bypass it. On the other hand, if the current is negative, the SM with the highest voltage will be conducted. This helps SM maintain an identical voltage level. However, sorting of all SMs at every sampling time brings in many unnecessary switching events, resulting in a very high average switching frequency, and correspondingly, a decreased conducting time.

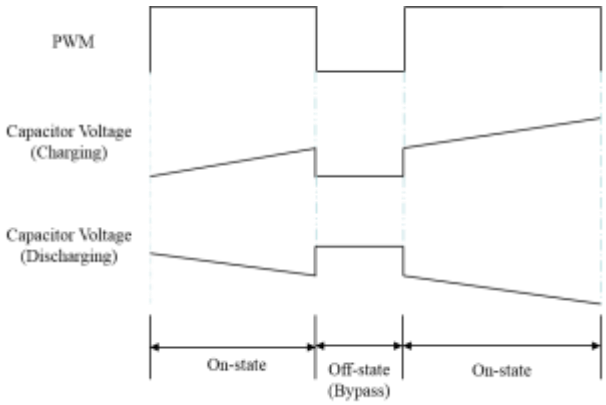

Figure 4. On/off state capacitor voltage waveform

III. THE PROPOSED CONDITION MONITORING APPROACH

A. *Reduced frequency sorting scheme*

Based on the previous analysis, the arm current i_x $(x = P\ or\ N)$ in Fig.3 flows through the sub-modules, so the capacitor current i_{cap} is represented as:

$$i_{cap} = S_x \cdot i_x \tag{1}$$

where S_x $(x = P\ or\ N)$ describes the switching state of SMs.

$$S_x = \begin{cases} 1, & ON - STATE \\ 0, & OFF - STATE \end{cases} \tag{2}$$

Fig.4 shows the typical voltage waveform across the SM capacitors. During the ON-STATE, the arm current either charges or discharges the capacitors, whereas during the OFF-STATE, the SM is bypassed and no arm current flows through the capacitor. Therefore, it is easier to describe the relationship between voltage and current during ON-STATE.

For the MMC system with a carrier frequency of 1 kHz to 2.5 kHz. The average ON-STATEs period is less than 2ms. With 20 kHz sampling frequency, normally 40 samples can be collected during one the ON-STATEs period which is insufficient for further condition monitoring, the condition monitoring method should either have fast convergence speed or less impact on the system operation [15]. Although this can be realized by combining two consecutive ON-STATEs period for parametric estimation, with the effect of leakage current, the accuracy of this method is not reliable. Therefore, this paper proposes an optimized control scheme for condition monitoring. It identifies a longer ON-STATEs period for acquiring and processing data samples, at the same time, having a minimum impact on the system operation. Fig.5 shows the proposed sorting scheme with combining the estimation approach, this can be described as follows:

a) Define the range of voltage ripple X (normally 5%), then apply sorting algorithms for m SMs that are outside of X.

b) If required SMs $n > m$, prioritize $(n - m)$ SMs based on the voltage reference, and then sort SMs that have higher priority.

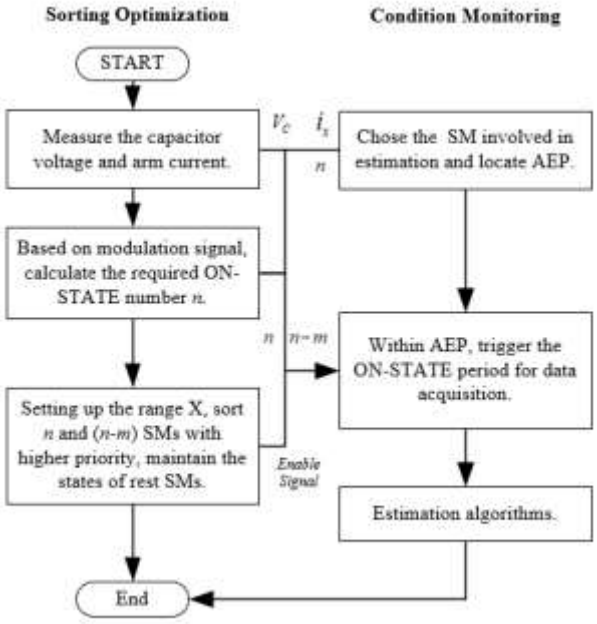

Figure 5. Proposed optimized sorting scheme with combining the estimation approach

c) Identify the available estimation period (AEP) from the lowest required SMs n (n = 0 or 1)

d) Trigger the ON-STATE period by comparing the voltage of selected SM with either the upper or lower limit of X, depending on the direction of arm current.

e) Collect voltage and current samples during ON-STATE period, implement the estimation algorithm.

Instead of accomplishing an identical SM voltage level in the conventional sorting algorithm that brings in unnecessary switching actions, the proposed sorting scheme operates the capacitor voltage within an acceptable range. The reduced switching frequency is greatly compatible with the condition monitoring. Most importantly, the range-based algorithm is designed to secure the ON-STATE period in AEP without sacrificing the output performance. It is worth noting that condition monitoring requires for a large set of samples, whereas the ON-STATE period is normally insufficient for most on-line estimation methods. Even with the proposed reduced frequency sorting scheme, an algorithm with fast convergence speed and high accuracy is required to achieve the best performance.

B. *Capacitor monitoring using fast-affine projection*

A simplified model of SM capacitor is shown in Fig.6 which consists of an inner capacitor and an equivalent series resistor. The voltage across the capacitor V_c is given as:

$$R_{ESR} \cdot S_x \cdot i_x + V_{cap} = V_c \tag{3}$$

V_{cap} is the instantaneous voltage of the inner capacitor which varies due to the charging and discharging process of the capacitor. With considering the switching states of SM in (1),

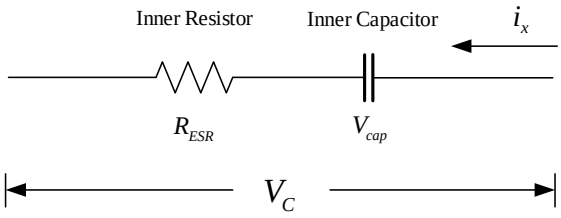

Figure 6. A simplified capacitor model

the relationship between the inner capacitor voltage and arm current is revealed as:

$$V_{cap} = \int \frac{S_x i_x}{C} \tag{4}$$

From (3) and (4), the capacitor equivalent circuit can be derived into a first-order differential equation (5), and its parameters can be estimated from the current and voltage at certain switching states.

$$\frac{R_{ESR}\, S_x\, di_x}{dt} + \frac{S_x i_x}{C} = \frac{dV_c}{dt} \tag{5}$$

Rather than interrupting the system operation using off-line methods [9, 16], this model is suitable for employing adaptive filter algorithms as they provide on-line parameter estimation. The capacitance C and resistance R_{ESR} can be identified by the current and voltage measurements which are readily available in the controller. With a sample time of T_s, the capacitor model (5) in Fig. 6 can be digitalized using zero-order holder:

$$Gz = \frac{R_{ESR} \cdot z + (\frac{T_s}{C} - R_{ESR})}{z-1} \tag{6}$$

Corresponding to (6), the target sub-module can be structured as a general discrete transfer function:

$$G(z) = \frac{bz+p}{z+a} = \frac{b+pz^{-1}}{1+az^{-1}} \tag{7}$$

a, b and p are the transfer function coefficients. Mapping (7) to (6), yield:

$$a = -1, b = R_{ESR}, p = \frac{T_s}{C} - R_{ESR} \tag{8}$$

where b and p are the coefficients to be estimated. The capacitance and ESR can then be obtained from the estimated coefficients.

Among adaptive algorithms, the fast-affine projection (FAP) has superior convergence speed and good estimation accuracy in the applications of parametric estimation. It uses the previous step calculation result in the current iteration to reduce the computational cost, thus providing a better convergence speed[17].

The way of implementing FAP algorithm for parametric estimation can be generally summarized as:

a) Determine the system structure (e.g. system order)

b) Determine the size of regressor and algorithm step size.

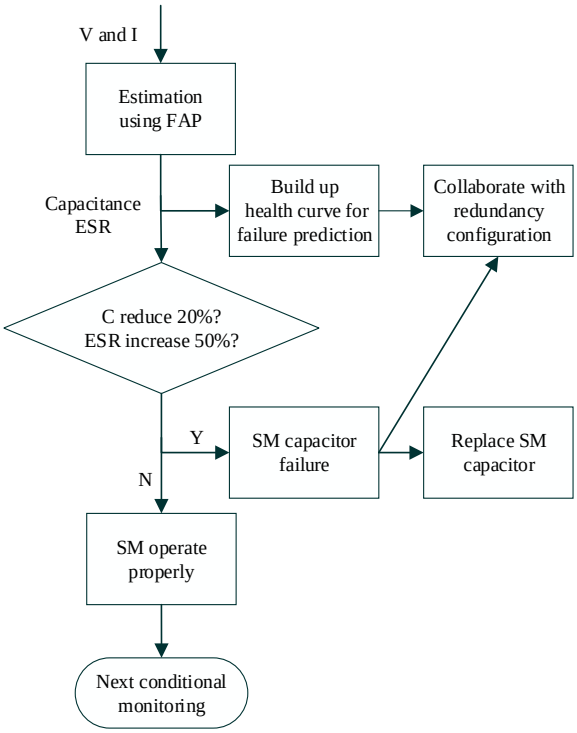

Fig 7. Proposed online condition monitoring in MMC applications

c) Start the estimation process, update the regressor matrices and the weight vector.

d) Repeat the iteration until the error is minimum, achieve an optimal set of transfer function coefficients.

e) Identify system parameters from estimated coefficients.

Fig.7 shows the flow chart of the proposed online condition monitoring approach in MMC application. The voltage and current measurements are processed by FAP, achieving a real-time estimation of ESR and capacitance when necessary. The process is repeated every certain period to get a capacitor condition curve that is used for failure prediction. The health monitoring approach can collaborate with the redundancy configuration, thus improving the system robustness. Besides, the capacitor failure can be detected by comparing the estimated parameters with the given datasheet. While there is a 20% decrease of capacitance or a 50% increase in ESR, the sub-module capacitor needs to be replaced.

IV. Simulation Results

An MMC model is developed in MATLAB to verify the performance of the proposed scheme. The model is supplied from a 6 kV DC source voltage with 4 SMs each arm, forming a 5-level voltage output. The modulation signals are obtained with the use of phase-shift pulse width modulation(PSPWM). The capacitor voltage and current are measured at a sampling frequency of 20 kHz. Table II summarizes the main system parameters.

TABLE II. Simulation parameters

Parameter	Value
Switching frequency	2 kHz
Arm inductance	1 mH
Load inductance	4 mH
Load resistance	30 Ω
SM capacitance	2000 μF
Capacitor ESR	0.4 Ω

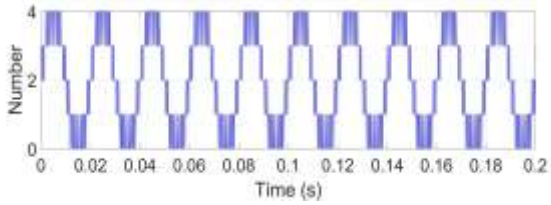

Figure 8. The required number of SMs for one arm based on PSPWM

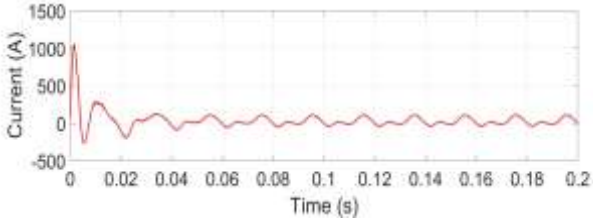

Figure 9. Upper arm current

Fig.8 shows the variations of the required number n within 10 cycles. The fundamental frequency is 50 Hz and the AEP appears from 240 degrees to 300 degrees. Fig 9 is the arm current of the upper arm, with the impact of dc component within the arm current, the average current is positive. During the AEP, in this case, the arm current is negative which means discharging the capacitors.

The comparison between the conventional sorting scheme and the optimized sorting scheme is shown in Fig. 10. It is obvious that the proposed sorting algorithm has better switching performance. The sorting event occurs within 0.2s decreased from 627 to 143, in other words, the average switching frequency has a 77.19% reduction, so the unnecessary switching frequency has been minimized significantly.

Based on the illustration in Section III, the range-based sorting scheme defines the upper and lower voltage limit based on the selected ripple range X, which in this case is set to 5%. The SM located inside the selected range has less possibility to change its switching states. In this simulation, when the current is positive and the required number is at the lower period between 0.075s to 0.080s, the trigger point is 0.078s when the SM1's voltage reaches the upper limit. Then for the next 25 sampling points, the switching state of SM1 is kept at ON-STATE. From the results in the Fig.11, the voltage selected estimation SM has small oscillation but still kept inside the selected range so the negative impact to the system

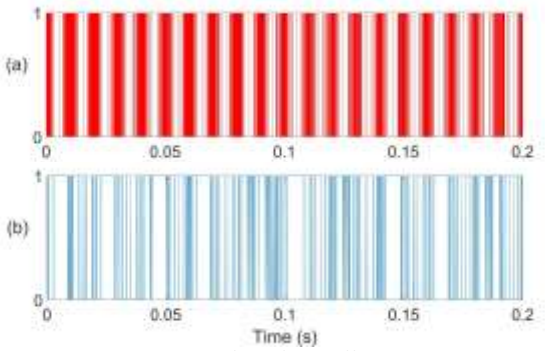

Figure 10. Switching states of SM from different sorting algorithms (a). Conventional sorting (b). Proposed reduced frequency sorting

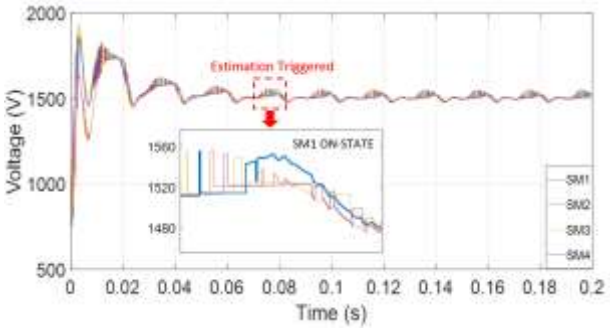

Figure 11. Capacitor voltage with applying the proposed estimation

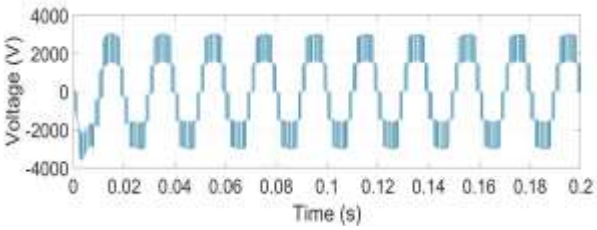

Figure 12. Output voltage with applying the proposed estimation

is negligible. The performance of the output voltage with the proposed scheme applied can be seen from Fig. 12, where no distortion in voltage level is observed when the estimation process is activated at 0.078s.

Fig.13 shows the effectiveness of FAP. In this case, the FAP used 20 to 25 point to get the estimated parameter of two coefficient b and p, the whole estimation time is less than 1.5ms. According to Fig 13, the value of coefficient b and p are 0.4125 and -0.3875 respectively. Compared the value of the estimated coefficient with the real value, the coefficient error of b is 3.13% and error of p 3.33%.

Based on (8), the ESR and capacitance of SM capacitor are identified from the estimated coefficients, which are 0.4125 Ω and 2000.0 μF as shown in Fig.14. Compared with the real value in 0.4 Ω and 2000.0 μF, the error of them is 3.3% and less than 0.01% accordingly. Table III summarizes a comprehensive overview of different capacitor monitoring approaches. Compared with other approaches, the proposed approach has huge improvement (90%) in accuracy and

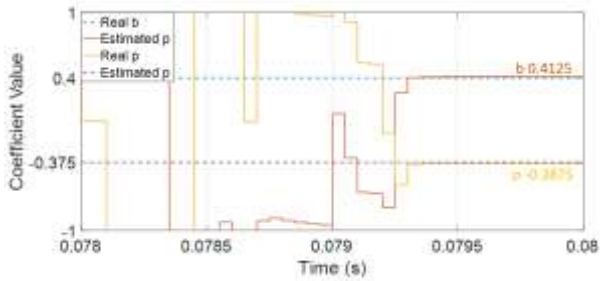

Figure 13. Transfer function coefficients estimation

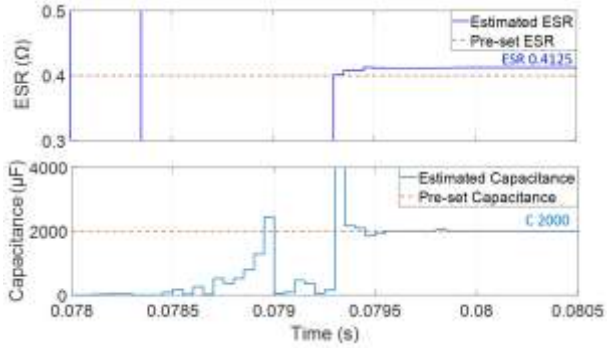

Figure 14. Condition monitoring of SM capacitor (ESR and C)

Table III. Comparison with existing approaches

Approaches	Estimation Time	Estimate Error of C	Extra Requirement
Signal injection with RLS[10]	15ms	1.3%	Extra source and filters.
C estimation using Kalman-filter[9]	400ms	2.0%	No
Calculated ripple-based impedance [8]	100ms	3.5%	Extra BPF
Proposed condition monitoring scheme	1.5ms	0.01%	No

response time as it requires the least samples to achieve the highest accuracy. Meanwhile, it requires no extra hardware or signal injection which distorts the system performance. In addition, the proposed approach can also estimate the ESR of the capacitor which is another critical indicator to assess the health of SM capacitor.

V. CONCLUSION

This paper presents an online condition monitor scheme for SM capacitors in MMC application by utilizing FAP with a compatible range-based reduced frequency sorting scheme. Compared with previous approaches, the proposed method not only performs evident advantages in terms of estimation accuracy and speed, but also maintain the system performance with reduced the switching events of SMs. In addition, it does not require for extra signal injection or hardware. From the simulation results, the convergence speed is less than 1.5 ms and the error is less than 3%. Due to its online characteristics, the proposed approach can be cooperatively implemented with redundancy management or utilized for monitoring the switching devices in MMC applications.

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