Reduced Order Model and Control of Non-Isolated High Gain Boost Converter

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***Abstract*—This paper present a reduced order model of interleaved boost converter integrating coupled inductor and switched capacitor by decoupling the leakage inductance leading to resonant exchange with the switched capacitors. State space averaging method is employed to derive the small signal ac model with ideal components. Furthermore, a dual loop control is adopted to regulate the output voltage of the converter. Extensive analysis and simulation demonstrate that the proposed model although simplified is sufficient for an adequate control system design ensuring fast transient response and good output voltage regulation.**

Keywords—High step-up DC-DC Converter, reduced order modelling, Control design, Coupled Inductor, Switched capacitor.

I. INTRODUCTION

Most of the devices that produce or store electrical energy (e.g. batteries, ultra-capacitors, fuel cells and solar photovoltaic PV) are built from low voltage sources which are usually connected in series to achieve desired voltage. Series connection of cells increases the system complexity and reduced performance due to manufacturing variation among cells and different working conditions. In addition, these sources also have a significant variation of their output voltages due to different state of charge (SoC) or the solar radiation [1].

Typical applications requires converters with high voltage gain, usually ten times or higher to harvest all available energy, which calls for high efficiency. These features have been the focus of many researches and huge number of topologies have proposed to this end.

Great effort has been devoted to dc-dc converter topologies fed by renewable sources, however, only few works have been found in modeling these converters. A dynamic model of six phase interleaved double dual boost and its control design is presented in [2]. Model investigation of three switching cell boost converter is described in [3], and the small signal model of current fed converter is presented in [4]. A full and reduced order model for the dc-dc multilevel boost converter based on state space averaging are proposed in [5]. The main reason being that most of the topologies have resonant stages or ripple that cannot be neglected in one or more state variables, which is key to requirement in applying state space averaging method.

This paper explore a topology proposed with the objective of realizing higher voltage gain in comparison with the conventional interleaved boost converter [6]. An interesting feature is that the power devices can be sized to a voltage lower than the output voltage. The main objective of this paper is to propose a reduced order model by excluding the leakage inductance of the coupled inductor which is inherent phenomena of the coupled inductor [1], [6], [7]. The paper presents a linearized dynamic model of interleaved boost converter integrating coupled inductor and switched capacitor. The result shows that the model differ from that of conventional interleaved couple inductor boost converter and the reduced order model is a good approximation of the system behavior.

II. CONVERTER DESCRIPTION AND ANALYSIS

Fig. 1 shows the two phase interleaved high step-up converter, where R_O represent the load and V_{in} and V_O represent the input and output voltages respectively. Each of the converter phase employs a coupled inductors and its corresponding pair of switch, clamp capacitor e.g. phase 1 comprises of coupled inductors L_1 switch S_1 clamp switch S_{C1}.and clamp capacitor C_{C1}. The primary winding of each coupled inductor e.g. L_{1a} is coupled to the corresponding secondary windings L_{1b}. The primary and secondary windings are denoted by n_1, n_2, and the coupling references denoted by ''o'' and ''*''. L_m denotes the magnetizing inductance of the coupled inductors whilst L_K represent the leakage inductances of the coupled inductors reflected to the secondary side. C_O denotes the output capacitor.

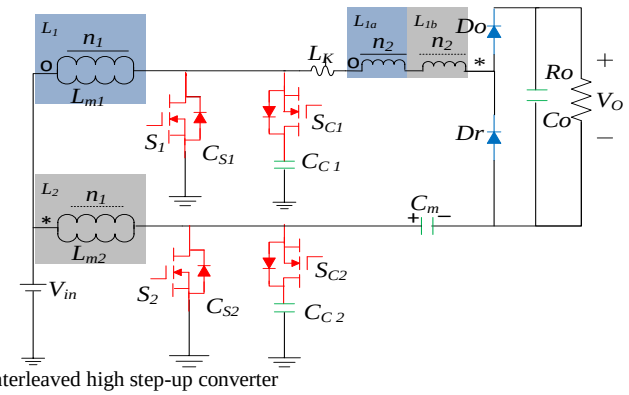

Fig. 1 Interleaved high step-up converter

During either of the main switch OFF instant, the voltage across the clamp and capacitors is denoted by

$$V_{Cc1} = V_{Cc2} = V_{in}/(1 - D) \quad (1)$$

When the power switch S_1 turns OFF the voltage across the switched capacitor and output voltage of the converter are

$$V_{Cm} = V_O/2 \tag{2}$$

$$V_O = V_{Cc1} + NV_{in} + N(V_{Cc1} - V_{in}) + V_{Cm} \tag{3}$$

Substituting (1) and (2) into (3), the voltage gain of the converter can be expressed as

$$M = \frac{V_O}{V_{in}} = \frac{2N+2}{(1-D)} \tag{4}$$

Where D is the converter duty is cycle and N is the coupled inductor turns ratio.

III. SMALL SIGNAL MODELLING

A typical interleaved converter operation is divided into four subintervals (switch ON and OFF instances). During each interval, the converter equations can be written in state space model of the form

$$\dot{x} = \begin{cases} A_1\mathbf{x} + B_1\mathbf{u} & S_1 and\ S_2\ on \\ A_2\mathbf{x} + B_2\mathbf{u} & S_1 on\ S_2\ off \\ A_3\mathbf{x} + B_3\mathbf{u} & S_1\ on\ \ S_2\ on \\ A_4\mathbf{x} + B_4\mathbf{u} & S_1 off\ S_2\ on \end{cases} \tag{5}$$

The state vector is defined in (6) by excluding the leakage inductance L_K to attain the average model and considering v_{Cm} as constant voltage source described by (2)

$$x = [i_{Lm1}\ i_{Lm2}\ v_{Cc1}\ \ v_{Cc2}\ v_O\ ]^T \tag{6}$$

and the input is defined as

$$u = [V_{in}] \tag{7}$$

Now assuming that the converter operate in continuous conduction (CCM) mode, no parasitic effect (i.e. neglecting short operating intervals), and switching frequency is much higher than the converter natural frequency. Equation (8)-(9)

$$\begin{cases} L_{m1}\dfrac{di_{Lm1}}{dt} = v_{in} \\ L_{m2}\dfrac{di_{Lm2}}{dt} = v_{in} \\ C_O\dfrac{dv_o}{dt} - \dfrac{v_o}{R_O} \end{cases} \tag{8}$$

$$\begin{cases} L_{m1}\dfrac{di_{Lm1}}{dt} = v_{in} \\ L_{m2}\dfrac{di_{Lm2}}{dt} = v_{in} - v_{Cc2} \\ v_{Cc2} = \dfrac{v_o}{2} + NL_{m2}\dfrac{di_{Lm2}}{dt} - Nv_{in} \\ C_O\dfrac{dv_o}{dt} = -\dfrac{v_o}{R_O} \end{cases} \tag{9}$$

$$\begin{cases} L_{m1}\dfrac{di_{Lm1}}{dt} = v_{in} - v_{Cc1} \\ L_{m2}\dfrac{di_{Lm2}}{dt} = v_{in} \\ v_{Cc1} = \dfrac{v_o}{2} + NL_{m1}\dfrac{di_{Lm1}}{dt} - Nv_{in} \\ C_O\dfrac{dv_o}{dt} = \dfrac{(1-d)i_{Lm1}}{(N+1)} - \dfrac{v_o}{R_O} \end{cases} \tag{10}$$

gives the state space equation during ON and OFF period. The use of state space averaging method [14] leads to the following set of differential equations that describe the converter dynamics

$$\begin{cases} L_{m1}\langle\dfrac{di_{Lm1}}{dt}\rangle = v_{in} - d'_{s1}v_{Cc1} \\ L_{m2}\langle\dfrac{di_{Lm2}}{dt}\rangle = v_{in} - d'_{s2}v_{Cc2} \\ C_{C1}\langle\dfrac{dv_{Cc1}}{dt}\rangle = i_{Lm1}d'_{s1} - \dfrac{T_s}{2L_k}((N+1)v_{Cc1} - \dfrac{v_O}{2})d'^{\,2}_{s1} \\ C_{C2}\langle\dfrac{dv_{Cc2}}{dt}\rangle = i_{Lm2}d'_{s2} - \dfrac{T_s}{2L_k}((N+1)v_{Cc2} - \dfrac{v_O}{2})d'^{\,2}_{s2} \\ C_O\langle\dfrac{dv_O}{dt}\rangle = \dfrac{(d'_{s1} + d'')i_{Lm1}}{(N+1)} - \dfrac{v_O}{R_O} \end{cases} \tag{11}$$

Where d_{s1}, d_{s2} are the duty cycles of main switch $S_1$and S_2 respectively. $d'_{s1} = (1 - d_{s1})$ $d'_{s2} = (1 - d_{s2})$, d'' is the period between the peak value of the leakage inductor current to its zero crossing during the positive half cycle and T_s is the switching time.

A. Steady State

The state space averaged DC model that describe the converter in equilibrium is obtained by letting the left-hand side (LHS) of (11) equal to zero, from which

$$\mathrm{X} = -A^{-1}BU \tag{12}$$

And the set of attainable equilibrium points are

$$\mathrm{x} = \begin{bmatrix} I_{Lm1} \\ I_{Lm2} \\ V_{Cc1} \\ V_{Cc2} \\ V_O \end{bmatrix} = \begin{bmatrix} \dfrac{2T_sV_{in}\,(N+1)^2}{4\,L_k(N+1) + R_oT_s(1+d^2+d'-2d-dd')} \\ \dfrac{2T_sV_{in}\,(N+1)^2}{4\,L_k(N+1) + R_oT_s(1+d^2+d'-2d-dd')} \\ V_{in}/(1-D) \\ V_{in}/(1-D) \\ \dfrac{2T_sV_{in}R_o(N+1)(1-d+d')}{4\,L_k(N+1) + R_oT_s(1+d^2+d'-2d-dd')} \end{bmatrix} \tag{13}$$

From (13), the non-ideal steady state voltage gain expression of the converter is given by

$$\frac{V_O}{V_{in}} = \frac{2T_sR_o(N+1)(1-d+d')}{4\,L_k(N+1) + R_oT_s(1+d^2+d^{'}-2d-dd^{'})} \tag{14}$$

The Laplace transfer function of the converter is derived from the state space model using (11) From which the line to output transfer function gives

$$G(s) = \begin{vmatrix} SI - A & -B \\ C & D \end{vmatrix} / |SI - A| \tag{15}$$

$$G_v(s) = \frac{V_o}{V_{in}}(s) = \frac{p_1 s + p_2}{s^3 + q_1 s^2 + q_2 s + q_3} \qquad (16)$$

Where $p_1 = (1 - d + d') \cdot s/(N+1)C_o L_m$, $p_2 = T_s(1-d)^2(1-d+d')/2L_k C_c L_m$, $q_1 = \frac{T_s(1-d)^2(N+1)}{2L_k C_c} + \frac{1}{R_o C_o}$ $q_2 = \frac{T_s(1-d)^2(N+1)}{2L_k C_c R_o C_o} + \frac{(1-d)^2}{L_m C_c}$, $q_3 = \frac{T_s(1-d)^2(1-d+d')}{4(N+1)L_m L_k C_c C_o} + \frac{(1-d)^2}{L_m C_c R_o C_o}$

The model in (16) is verified with direct simulation with switch model under full load condition. Fig. shows the simulated and calculated model.

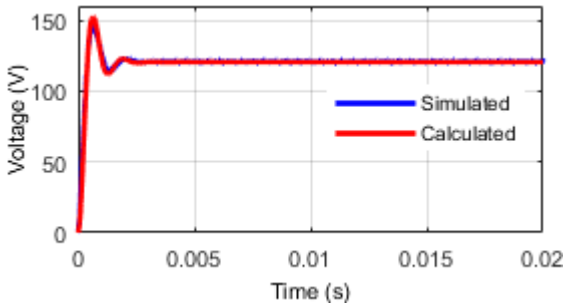

Fig. 2 Switch and calculated model validation

B. Perturbation and Linearization

A linearized system can be developed by introducing perturbation around the steady state value of the averaged model calculated in (11), containing the steady state dc value represented by uppercase letter and a superimposed ac variation represented by lowercase symbol with circumflex [8-11]. For instance the perturbation definitions for the state variable are: $i_{Lm} = I_{Lm} + \hat{\imath}_{Lm}$, $v_{in} = V_{in} + \hat{v}_{in}$, $v_o = V_o + \hat{v}_o$ and $d = D + \hat{d}$. Then by expanding and neglecting the higher order perturbation terms, then removing the steady-state quantities gives the small signal ac model of the converter.

$$\begin{cases} L_{m1}\frac{d(I_{Lm1}+\hat{\imath}_{Lm1})}{dt} = V_{in} + \hat{v}_{in} - (V_{Cc1} + \hat{v}_{Cc1})(1 - D - \hat{d}_{s1}) \\ L_{m2}\frac{d(I_{Lm2}+\hat{\imath}_{Lm2})}{dt} = V_{in} + \hat{v}_{in} - (V_{Cc2} + \hat{v}_{Cc2})(1 - D - \hat{d}_{s2}) \\ C_{C1}\frac{d(V_{Cc1}+\hat{v}_{Cc1})}{dt} = (I_{Lm1} + \hat{\imath}_{Lm1})(1 - D - \hat{d}_{s1}) \\ -\frac{T_s(1 - D - \hat{d}_{s1})^2}{2L_k}\left((N+1)(V_{Cc1} + \hat{v}_{Cc1}) + \frac{(V_o + \hat{v}_o)}{2}\right) \\ C_{C2}\frac{d(V_{Cc2}+\hat{v}_{Cc2})}{dt} = (I_{Lm2} + \hat{\imath}_{Lm2})(1 - D - \hat{d}_{s2}) \\ -\frac{T_s(1 - D - \hat{d}_{s2})^2}{2L_k}\left((N+1)(V_{Cc2} + \hat{v}_{Cc2}) + \frac{(V_o + \hat{v}_o)}{2}\right) \\ C_o\left\langle\frac{d(V_o+\hat{v}_o)}{dt}\right\rangle = \frac{I_{Lm1}+\hat{\imath}_{Lm1}}{(N+1)}(1 - D - \hat{d}_{s1} + D' + \hat{d}') \\ \qquad - \frac{(V_o + \hat{v}_o)}{R_o} \end{cases} \qquad (17)$$

C. Order Reduction

Considering a perfect symmetry among the phases of the converter such that all the components are exactly the same, the duty cycle of the main switches are the same and that of corresponding clamp switches are also similar i.e.

$$\begin{cases} L_{m1} = L_{m2} = L_m \\ C_{C1} = C_{C2} = C_C \\ d_{s1} = d_{s2} = d_s \end{cases} \qquad (18)$$

In addition, the voltage across clamp capacitors are equal $V_{Cc1} = V_{Cc2} = V_{Cc}$ and there is equal current sharing between the converter phases exist such that $i_{Lm1} = i_{Lm2} = i_{Lm}$, $i_{Lm1} + i_{Lm2} = i_{In}$. When these condition are taking into account the fifth order equation in (17) can be written as

$$\begin{cases} L_m\frac{d\hat{\imath}_{in}}{dt} = 2\hat{v}_{in} - V_{Cc}\hat{d} - 2(1-D)\hat{v}_{Cc} \\ C_C\left\langle\frac{dv_{Cc}}{dt}\right\rangle = (1-D)\hat{\imath}_{Lm} - I_{Lm}\hat{d} - \frac{T_s(1-D)^2}{2L_k}. \\ \left((N+1)\hat{v}_{Cc} - \frac{\hat{v}_o}{2}\right) + \frac{T_s(1-D)\hat{d}}{L_k}\left((N+1)V_{Cc} - \frac{V_o}{2}\right) \\ C_o\frac{d\hat{v}_o}{dt} = \frac{\hat{\imath}_{in}(1-D+D')}{2(N+1)} - \frac{I_{Lm}\hat{d}}{2(N+1)} + \frac{I_{Lm}\hat{d}'}{(N+1)} - \frac{\hat{v}_o}{R_o} \end{cases} \qquad (19)$$

Taking Laplace transform of (19) and replacing s with d/dt. Then eliminating $\hat{d}'$ yield the small signal low-frequency model of the interleaved high step-up converter.

$$\begin{cases} s\cdot L_m\cdot\hat{\imath}_{in}(s) = 2\hat{v}_{in}(s) - V_{Cc}\hat{d}(s) - 2(1-D)\hat{v}_{Cc}(s) \\ s\cdot C_c\cdot\hat{v}_{Cc}(s) = (1-D)\hat{\imath}_{Lm}(s) - I_{Lm}\hat{d}(s) - \frac{T_s(1-D)^2}{2L_k}.. \\ \left((N+1)\hat{v}_{Cc}(s) - \frac{\hat{v}_o(s)}{2}\right) + \frac{T_s(1-D)\hat{d}(s)}{L_k}\left((N+1)V_{Cc} - \frac{V_o}{2}\right) \\ sC_o\hat{v}_o(s) = \frac{\hat{\imath}_{in}(s)(1-D+D')}{2(N+1)} - \frac{I_{Lm}\hat{d}(s)}{2(N+1)} + \frac{I_{Lm}\hat{d}'(s)}{(N+1)} - \frac{\hat{v}_o(s)}{R_o} \end{cases} \qquad (20)$$

From (19) the system matrix can be written as

$$A = \begin{bmatrix} s & \frac{2(1-D)}{L_m} & 0 \\ -\frac{(1-D)}{C_c} & s + \frac{(N+1)(1-D)^2}{2f_s L_k C_c} & -\frac{(1-D)^2}{4L_k C_c} \\ -\frac{(1-D+D')}{2(N+1)C_o} & \frac{2I_{Lm}(1-D)}{C_o V_o} & s + \frac{1}{R_o C_o} + \frac{2I_{Lm}(1-D+D')}{(N+1)C_o V_o} \end{bmatrix}$$

$$B = \left[\frac{2V_{Cc}}{L_m}, \frac{(1-D)\left((N+1)V_{Cc} - \frac{V_o}{2}\right)}{f_s L_k C_c} - \frac{I_{Lm}}{C_c}, -\frac{2I_{Lm}V_{Cc}}{V_o C_o}\right]^T, \quad C = \begin{pmatrix} 0 \\ 0 \\ 1 \end{pmatrix}$$

Following this various transfer functions can be derived suitable for closed loop control system design of the converter

$$\begin{bmatrix} \hat{\imath}_{in}(s) \\ \hat{v}_{CC}(s) \\ \hat{v}_o(s) \end{bmatrix} = [A(s)]^{-1}\begin{bmatrix} b_1(s) \\ b_2(s) \\ b_3(s) \end{bmatrix}\hat{d}(s) + [A(s)]^{-1}[C(s)]\hat{v}_{in}(s) \qquad (21)$$

D. Duty Ratio Control

Direct duty ratio control is obtained by making $\hat{v}_{in}(s) = 0$ in (21) given by

$$G_{vd}(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{a_1 s^2 + a_2 s + a_3}{p_1 s^3 + p_2 s^2 + p_3 s + p_4} \qquad (22)$$

Where $a_1 = L_m C_c b_1$, $a_2 = \frac{(1-D+d')C_c}{2(N+1)}\cdot b_1 + \frac{2I_{Lm}L_m(1-D)}{V_o}\cdot b_2 + \frac{(1-D)^2 L_m}{f_s L_K}\cdot b_3$

$a_3 = (1-D)^2\left(\frac{(1-D+D')}{2f_s L_K} + \frac{2I_{Lm}(1-D)}{V_o}\right)\cdot b_1 - \frac{2(1-D+D')(1-D)}{(N+1)}\cdot b_2 +$

$$2(1-D)^2 \cdot b_3, , p_2 = \frac{L_m C_O (1-D)^2}{f_s L_K} + L_m C_c \left(\frac{1}{R_O} + \frac{2I_{Lm}(1-D+D')}{(N+1)V_o}\right),$$

$$p_1 = L_m C_c C_O,\ p_3 = \frac{L_m (1-D)^2}{f_s L_K}\left(\frac{1}{R_O} + \frac{2I_{Lm}(1-D+D')}{(N+1)V_o}\right) + 2C_O(1-D)^2,$$

$$p_4 = 2(1-D)^2\left(\frac{1}{R_O} + \frac{2I_{Lm}(1-D+D')}{(N+1)V_o} + \frac{(1-D)(1-D+D')}{f_s L_K (N+1)^2}\right)$$

Where D' represents the steady state dc value of d'.

The control-to-output transfer function describes a standard third order system and has a negative real pole at $s = -5.65e05$, two complex conjugate poles at $s = -7.57 \pm j1.3e03$, and two zeros at $s = -5.65e05$ and $s = 1.34e04$ respectively. The control-to-output transfer function exhibit a non-minimum phase system, which is typical behaviour of converters with boost or buck-boost characteristics.

The control-to-output transfer function in (22) is once again verified in simulation by perturbing duty cycle set point with sinusoids of different frequencies and stores the corresponding output voltage. A discrete points are obtained from the frequency response that describes how the system responds to the magnitude and phase of the injected sinusoids. In essence, the control-to-output transfer function can be estimated from the measured data. Fig. 3 illustrates the Bode plot of both the calculated and estimated response of the control-to-output transfer function. As can be seen a good agreement exist between the models and the calculated model is suitable for the frequency domain analysis and controller design. The parameters of the simulation and the calculated model are listed in Table I.

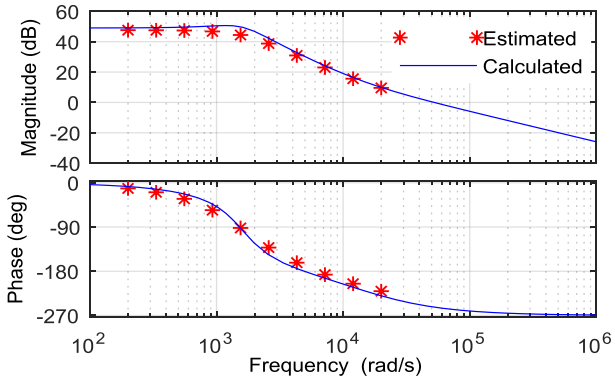

Fig. 3 Calculated and estimated control to output transfer function

TABLE I. CONVERTER PARAMETERS

Parameter	Rating
Output Power (P_O)	500 W
Input Voltage (V_{in})	12 V
Output Voltage (V_O)	120 V
Switching Frequency (f_s)	50 KHz
Clamp capacitors (C_c)	4.7 µF
Switched Capacitor (C_m)	10 µF
Output capacitor (C_O)	50 µF
Turns Ratio (n_2/n_1)	1:1
Magnetizing Inductance (L_m)	36 µH

IV. CONTROLLER DESIGN

Fig. 4 illustrates the block diagram of the control strategy used to investigate the closed loop dynamic performance of the converter. It is a typical dual loop control, comprising of inner current loop and outer voltage loop. The presence of the right half plane (RHP) zero in the control-to-output transfer function of (21) tends to destabilize the single-loop feedback control. It is difficult to obtain an adequate phase margin (PM), because during transient the phase lag of the right (RHP) zero causes the output to change initially in the wrong direction [12]. The loops are usually defined to satisfy certain design criteria of PM and bandwidth.

The feedback control system uses proportional-integral (PI) controller in both loops. The outer voltage loop determines the current reference of the inner current loop, whilst the control signal is determined by the inner current controller. The control signal generates the gating signals of the main switches S_1 and S_2 with the same duty ratio with the aid of digital pulse width modulation (DPWM) submodule. Two modulators shifted in phase by 180^0 are used to produce the gating signals. Note that the gate signal of the clamp switches S_{C1} and S_{C2} are complementary to their corresponding primary switches. The current and voltage transducers have been taken into account with their respective gains H_i, H_v.

The outer voltage loop has slow dynamics whilst the inner current loop has fast dynamics. This is to allow the input current to respond more quickly than the converter output voltage. The DPWM module in Fig. 5 comprises of the Padè approximation block and the moldulator static gain [12].

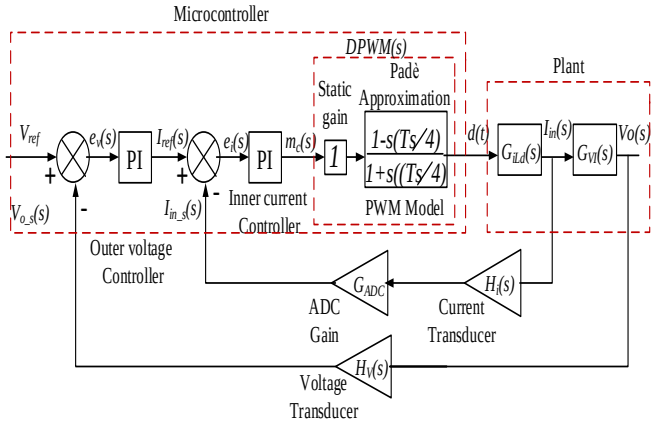

Fig. 4 Block diagram of current mode control

A. Inner Current Control Loop

From Fig. 4, the inner current PI controller is designed first, using the control to input current transfer function from (23)

$$G_{id}(s) = \frac{\hat{i}_{in}(s)}{\hat{d}(s)} = \frac{q_1 s^2 + q_2 s + q_3}{p_1 s^3 + p_2 s^2 + p_3 s + p_4} \qquad (23)$$

Where

$$q_1 = b_1 \cdot s^2 + \left(\frac{1}{R_O C_O} + \frac{(N+1)(1-D)^2}{2f_s L_K C_c} + \frac{2I_{Lm}(1-D+D')}{(N+1)V_o}\right) \cdot b_2\ s$$
$$+ \frac{(N+1)(1-D)^2 \cdot b_3}{2f_s L_K C_c}\left(\frac{1}{R_O C_O} + \frac{2I_{Lm}(1-D+D')}{(N+1)V_o}\right) + \frac{2I_{Lm}(1-D)^3}{4f_s L_k C_c C_o V_o} \cdot b_3$$

$$q_2 = -2(1-D)Co \cdot b_1 - 2(1-d)\left(\frac{1}{R_O} + \frac{2I_{Lm}(1-D+D')}{(N+1)V_o}\right) \cdot b_2$$

$$q_3 = -\frac{(1-D)^3}{(N+1)f_s L_K} \cdot b_3$$

Following this, the open loop transfer function of the inner current control loop (simply a cascade connection of all blocks)

is required to design the controller. This transfer function is given by

$$G_{oL}(s) = \frac{K_p(s+K_i/K_p)}{s} \cdot \frac{(1-s\,T_s/4)}{(1+s\,T_s/4)} \cdot H_i(s) \cdot G_{id}(s) \qquad (24)$$

Where $H_i(s)$ is the current sensor gain. The continuous time system in (24) is first discretized with zero order hold (ZOH) given by

$$G_{id}(z) = Z\{\frac{1}{s}(1-e^{-sTs})H(s) \cdot G_{id}(s)\} \qquad (25)$$

Once this is available, the digital PI controller is designed directly in the discrete time domain using methods similar to continuous time frequency response. The compensator design is driven by certain specifications concerning the closed loop performance (such as speed of response or tracking error with respect to the reference signal). For this reason, a closed loop bandwidth f_{CL} of one tenth of the switching frequency f_s is intended to be achieved with at least PM of 60^o. The subsequent step is to determine the proportional gain K_p and integral gain K_I that guarantee compliance with these specifications. Fig. 5 illustrate the Bode diagram of the inner

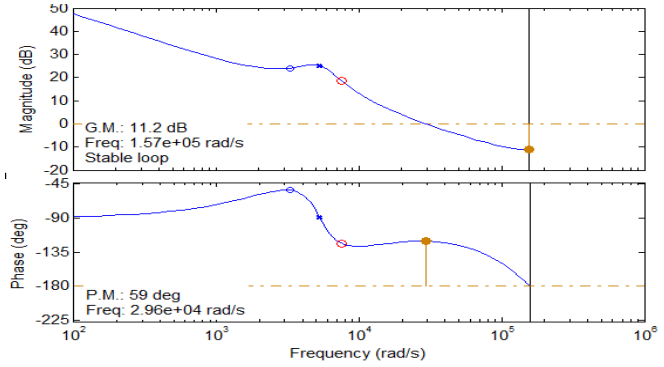

Fig. 5 Control to duty cycle transfer function Bode diagram

current loop, showing compliance with design specifications. The controller is designed in Matlab using a "sisotool" graphical user interface based on Zeigler-Nichols tuning that allows the closed loop frequency response to be interactively changed by modifying the pole-zero location of the PI compensator. The corresponding feedback compensator gains from the same interface are $K_p = 0.0151$ and $K_I T_s = 0.0025$ respectively.

B. Outer Voltage Loop

The outer voltage PI controller is design in similar way using the voltage to current transfer function (26)

$$G_{vi}(s) = \frac{\hat{v}_o(s)}{\hat{I}_{in}(s)} = \frac{a_1 s^2 + a_2 s + a_3}{q_1 s^2 + q_2 s + q_3} \qquad (26)$$

Where $a_1 = L_m C_c b_1$, $a_2 = \frac{(1-D+d')C_c}{2(N+1)} \cdot b_1 + \frac{2I_{Lm}L_m(1-D)}{V_o} \cdot b_2 + \frac{(1-D)^2 L_m}{f_s L_K} \cdot b_3$

$a_3 = (1-D)^2\left(\frac{(1-D+D')}{2f_s L_K} + \frac{2I_{Lm}(1-D)}{V_o}\right) \cdot b_1 - \frac{2(1-D+D')(1-D)}{(N+1)} \cdot b_2 + 2(1-D)^2 \cdot b_3$, $q_1 = b_1 \cdot s^2 + \left(\frac{1}{R_O C_O} + \frac{(N+1)(1-D)^2}{2f_s L_K C_c} + \frac{2I_{Lm}(1-D+D')}{(N+1)V_o}\right) \cdot b_2\, s +$

$\frac{(N+1)(1-D)^2 \cdot b_3}{2f_s L_K C_c}\left(\frac{1}{R_O C_O} + \frac{2I_{Lm}(1-D+D')}{(N+1)V_o}\right) + \frac{2I_{Lm}(1-D)^3}{4f_s L_K C_c C_o V_o} \cdot b_3$, $q_3 = -\frac{(1-D)^3}{(N+1)f_s L_K} \cdot b_3$

$q_2 = -2(1-D)Co \cdot b_1 - 2(1-d)\left(\frac{1}{R_O} + \frac{2I_{Lm}(1-D+D')}{(N+1)V_o}\right) \cdot b_2$,

The open loop gain is given by

$$G_{oL}(s) = \frac{K_p(s+K_i/K_p)}{s} \cdot H_v(s) \cdot G_{vi}(s) \qquad (27)$$

Where $H_v(s)$ is the voltage transducer gain. To ensure sufficient stability around equilibrium point due to parameter variation influence, a closed loop bandwidth f_{CL} of one tenth of the inner current loop is intended to be achieved with at least phase

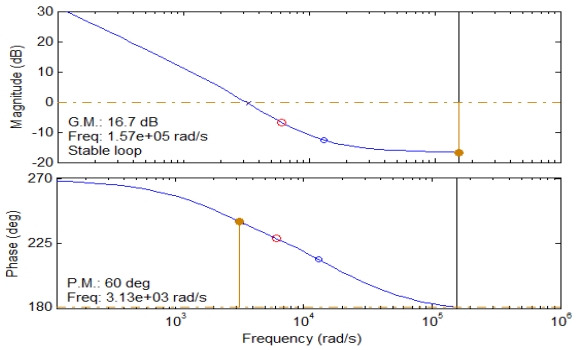

Fig. 6 Bode diagram of voltage control loop with discrete PI controller

margin PM of 60^o. Following the same method described in the current loop the proportional gain K_p and integral gain K_I of the voltage loop that guarantees compliance with these specifications are $K_p = 0.1987$ and $K_I T_s = 0.00258$ respectively. Fig. 6 shows the Bode plot of the voltage control loop with the discrete controller. The desired specifications of phase and gain margins were achieved and the low-frequency gain is improved.

V. Simulation Results

To verify the theoretical analysis and the closed loop dynamics performance of the converter. A 500 W is designed and built in Matlab/Simulink with the parameters listed in Table I. The transient response characteristics such as settling time, peak over shoot and steady state error for output voltage regulation during the load perturbation are observed. Fig. 7 and Fig. 8 shows the simulated response of the converter due to load disturbances.

In Fig. 7, a step change in load resistance is applied, causing a step decrement in output power from 500 W to 100 W and vice versa. The peak overshoot is 20% of the steady state output voltage and the settling time is 30ms. Another load disturbance is applied in Fig. 8, causing a step decrement in output power from 250 W to 400 W and vice versa. Unlike the previous case, the output response settle faster within 15ms and the overshoot/undershoot reduces to 6.6% of the steady state values

VI. Conclusion

The derivation of the reduced order small signal model of interleaved high step-up converter with coupled inductors and switched capacitor in CCM is presented in this paper. The validity of the derived model is verified in simulation and used in the design of the dual loop controllers. The dynamic response of the converter under the influence of the designed PI

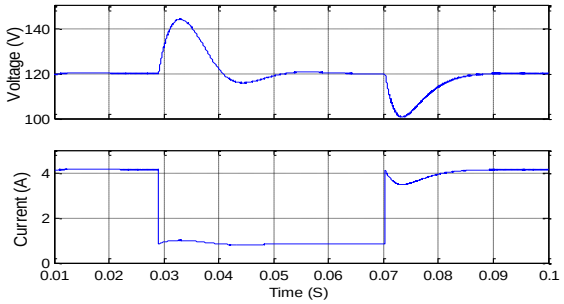

Fig. 7 Step change in load from full load down to 20% load

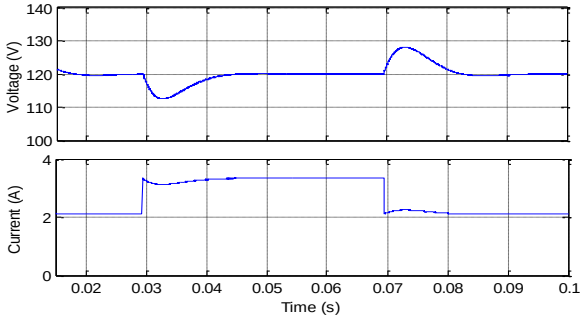

Fig. 8 Load change from half load to 80% load

controllers during load disturbance is also verified via a simulation. The proposed reduced order model exhibits good transient response during disturbances and adequate for controller design capable of good voltage regulation and disturbance rejection.

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