Olsen SH, O'Neill AG, Bull SJ, Woods NJ, Zhang J.

[Effect of metal-oxide-semiconductor processing on the surface roughness of strained Si/SiGe material](http://dx.doi.org/10.1063/1.1489712).

Copyright:

DOI link to article:

http://dx.doi.org/10.1063/1.1489712

Date deposited:

15/09/2016

Effect of metal–oxide–semiconductor processing on the surface roughness of strained Si/SiGe material

S. H. Olsen[a] and A. G. O'Neill
Department of Electrical and Electronic Engineering, University of Newcastle, Newcastle upon Tyne, NE1 7RU, United Kingdom

S. J. Bull
Department of Mechanical, Materials and Manufacturing Engineering, University of Newcastle, Newcastle upon Tyne, NE1 7RU, United Kingdom

N. J. Woods and J. Zhang
Department of Physics, Centre for Electronic Materials and Devices, Imperial College of Science, Technology and Medicine, Prince Consort Road, London, SW7 2BW, United Kingdom

The impact of metal–oxide–semiconductor processing on strained Si/SiGe device structures has been examined. Material was grown by gas-source molecular beam epitaxy and ultra low pressure chemical vapor deposition, with different as-grown surface roughness. The effects of RCA cleaning, gate oxidation and rapid thermal annealing on this material were studied by atomic force microscopy (AFM) and optical profilometry. Certain processes caused reactions common to both material types, whereas others yielded dissimilar responses. Filtering AFM roughness data of specific wavelengths enabled the effects of processing on large-scale surface roughness dominated by the cross-hatching morphology and smaller scale microroughness to be investigated. The results suggest that as-grown Si/SiGe material quality is not a good indicator of processed device performance, rather morphological changes which occur during processing must be considered. © 2002 American Institute of Physics. [DOI: 10.1063/1.1489712]

I. INTRODUCTION

In 1965, Gordon Moore successfully predicted that the performance of integrated circuits would double every 18–24 months. This prediction has largely been achieved in complementary metal–oxide–semiconductor (CMOS) technology through the aggressive scaling of device dimensions and in particular, an exponential decrease in transistor gate length with each technology generation. While further performance enhancements remain possible using current Si technology, increasing design and fabrication costs for new technology generations may make them prohibitive.[1] Thus, alternative materials with advanced properties for mainstream applications are actively being sought. The Si/SiGe material system is presently receiving widespread attention due to its successful integration into bipolar technology[2] and, with its incorporation into CMOS technology, the promise of even greater performance advantages compared with conventional Si[3,4] without the high costs associated with geometric scaling. The clear benefit of the strained Si/SiGe system compared with other advanced material systems is its compatibility with conventional Si fabrication techniques. This has recently led to the addition of strained Si/SiGe as a key emerging research technology in the *2001 International Technology Roadmap for Semiconductors*.[5]

There is a 4.2% lattice mismatch between Si and Ge. When Si is epitaxially grown on relaxed SiGe, the Si becomes strained and acquires a reduced electron effective mass in the transport direction.[3] By causing the Si to be strained, band degeneracy is lifted, reducing intervalley scattering and increasing electron mobility. If such a strained Si layer is used as the electron channel of a field-effect transistor, it would be anticipated that increased mobility would lead to performance enhancement.[3,4]

While theoretically predicted mobilities have been demonstrated experimentally in strained Si/SiGe *n*-channel heterojunction modulation-doped field-effect transistor (MODFET) structures operating at room temperature,[6] the performance of strained Si/SiGe *n*-channel heterojunction MOSFETs (HNMOSFETs) fabricated on both gas-source molecular beam epitaxy (GS-MBE) material[7] and chemical vapor deposition (CVD) material[8] has been somewhat lower than in theory. Since MODFET devices require far less processing than MOSFETs, the degradation in HNMOSFET performance appears to be caused by device fabrication, and in particular, the difference between MOSFET and MODFET processing.

For all types of MOS surface channel devices, the Si/SiO$_2$ interface quality is paramount, since it is against this interface that the inversion layer and carrier conduction occur and carrier scattering from roughness at the oxide interface is a principal mobility limiting mechanism.[9–11] Strained Si/SiGe buried channel device designs may overcome the effects of oxide interface scattering, but the loss in transconductance for a channel further beneath the gate proves dominant and maximum performance advantages are predicted

[a]Electronic mail: sarah.olsen@ncl.ac.uk

     1298

from strained Si surface channel devices.[12] Therefore, in order to realize the potential of strained Si/SiGe MOS devices, precise control of the Si/SiO_2 interface, and thus the surface roughness, is essential.

The present study examines the effects of device processing on the surface roughness of strained Si/SiGe MOS architectures. GS-MBE and ultra low pressure chemical vapor deposition (ULPCVD) growth techniques were used to produce strained Si/SiGe material with differing as-grown morphology in order to investigate whether the roughness of as-grown material is a suitable indicator for predicting device performance. The impact of RCA cleaning, gate oxidation and rapid thermal annealing (RTA) on surface roughness of strained Si/SiGe has been studied using atomic force microscopy (AFM) and optical surface profiler techniques. Electrical data on these part processed samples is not available, but a recent study has suggested that the electrical performance of fully processed devices is influenced by the Si/SiGe morphology.[13]

Roughness correlation lengths known to affect conventional Si device mobility can be analyzed using the two dimensional (2D) power spectra of AFM roughness since roughness is considered isotropic on Si surfaces.[14,15] However, relaxed SiGe exhibits characteristic cross-hatching roughness that arises due to the misfit dislocation network in the relaxed alloy and the variation in growth with strain fluctuations.[16–18] These prominent undulations are repeated through subsequent epitaxial layer growths,[19] thus the morphology becomes evident at the Si/SiO_2 interface of strained Si/SiGe surface channel devices. The cross-hatch morphology of strained Si/SiGe material has been found to display anisotropies of both roughness amplitudes and lateral correlation lengths, depending on whether they are measured along or diagonal to the cross-hatch pattern.[19] Therefore fast Fourier transforms of AFM data, allowing 3D spectral analyses of roughness, were considered more suitable for investigating Si/SiGe material. Signal filtering techniques have additionally been employed to differentiate between the effects of MOSFET processing on large-scale cross-hatching and roughness at smaller wavelengths likely to affect carrier transport. The variation in cross-hatch roughness across the wafers has also been analyzed.

The study found that despite a difference in the as-grown quality of material produced by GS-MBE and ULPCVD, the surface roughness of high alloy composition Si/SiGe material grown by both methods deteriorated with high thermal budget processing. Low temperature RCA cleaning did not lead to such degradation, suggesting that the weak performance gains observed in strained Si/SiGe HNMOSFET devices arises from the high thermal budget used during fabrication. The greater performance enhancements of strained Si/SiGe MODFET devices over conventional Si are considered to be attributed to the significantly lower thermal budget required for MODFET fabrication. The results demonstrate that morphology of as-grown Si/SiGe material is an inadequate indicator for predicting surface channel HNMOSFET device performance, rather the surface roughness following processing should be considered.

TABLE I. Single RCA cleaning procedure.

Process step	Chemicals	Mixing ratios
1 (RCA1)	$H_2O:NH_4OH:H_2O_2$	5.3:1.4:1.0
2	DIH_2O	...
3 (RCA2)	$H_2O:HCl:H_2O_2$	6.6:1.0:1.0
4	DIH_2O	...

II. EXPERIMENTAL DETAILS

The experiments were carried out on two types of Si/SiGe material. The first wafer was grown using conventional GS-MBE methods[20,21] with fluxes of dilsilane (Si_2H_6) and germane (GeH_4). The temperature was maintained at 550 °C throughout growth, and the pressure of the system was in the range $10^{-5}–10^{-4}$ Torr. The as-grown layer structure of the GS-MBE wafer was measured by transmission electron microscopy (TEM) and the alloy composition determined by x-ray diffraction analysis (XRD). An 11.5 nm strained Si layer was grown on a 1400 nm $Si_{0.67}Ge_{0.33}$ relaxed virtual substrate (VS). The VS was grown on a graded $p^- Si_{1-x}Ge_x$ layer with x gradually increasing from 0 to 0.32. Growth of the graded alloy and the VS required 27 h. XRD verified that the VS was 98.9% relaxed. The critical thickness for Si on relaxed $Si_{0.67}Ge_{0.33}$ is approximately 10 nm[22] and RCA cleaning ensured that the Si thickness was below this thickness prior to subsequent high temperature processing steps.

The graded $p^- Si_xGe_{1-x}$ alloy and the relaxed SiGe VS of the second wafer used in this study were grown using the ULPCVD method[20] at 550 °C. Although the technique was carried out at a very low pressure (roughly $10^{-2}–10^{-1}$ Torr) compared with conventional CVD processes, the pressure is much higher than that used in GS-MBE, enabling growth in approximately 4.5 h, significantly less than for the GS-MBE wafer. A 10 nm strained Si layer [measured by TEM and secondary ion mass spectroscopy (SIMS)] was grown above the VS in the conventional GS-MBE mode at 600 °C. XRD confirmed that the VS was 99.3% relaxed and that the Ge composition was 30.3%, in good agreement with the value of 28% obtained using SIMS (data not shown).

Samples of the GS-MBE and ULPCVD wafers were subjected to two RCA cleaning procedures as would be carried out prior to gate oxidation in a standard MOSFET process. The first is carried out at the start of fabrication to remove any surface contaminants. The second is carried out immediately before the gate oxidation to ensure the removal of organic and metallic particulates, which may adversely affect device threshold voltages. The mixing ratios for the chemicals used in the RCA procedure are shown in Table I. The primary role of RCA1 is surface particulate removal using dilute ammonium hydroxide/hydrogen peroxide (NH_4OH/H_2O_2) etching. A de-ionized (DI) water rinse was subsequently carried out, which was superseded by the RCA2 clean. The dilute hydrochloric acid/hydrogen peroxide $(HCl)/(H_2O_2)$ mixture used in RCA2 is effective at controlling metallic contamination. RCA2 was followed by an additional DI rinse. The second RCA cleaning sequence was carried out immediately after the first.

TABLE II. Oxidation conditions.

Oxidation process	Temperature (°C)	Time (min)	Ambient
O_2_high	800	120	O_2
O_2_medium	800	60	O_2
O_2_low	750	60	O_2

All samples subjected to thermal treatments were the same size (one-eighth segments of a 4-in. wafer) to avoid any differences in the heat distribution across the samples. Dry furnace oxidations were performed on samples from the GS-MBE wafer, the ULPCVD wafer and Si control wafers, all samples having first undergone two RCA cleans, as experienced by the material during the fabrication of devices. Details of the oxidation processes are given in Table II. The overall thermal budget and ambient to which the samples were exposed are indicated in the sample names. The O_2_high oxidation was carried out in O_2 at 800 °C for 120 min. The O_2_medium oxidation was carried out at 800 °C for 60 min. In addition, a sample from the ULPCVD wafer underwent a low thermal budget oxidation for 60 min at 750 °C (O_2_low). The resulting oxide was not etched before measuring roughness because the surface microroughness of thin oxides, such as those arising from the oxidations performed in the present experiments, is equivalent to that of the underlying Si/SiO_2 interface.[23] Oxidations were performed in the absence of HCl and all samples received a 15 min post-oxidation anneal in N_2 at the oxidation temperature. Although the increase in thermal budget from the N_2 anneal is important with respect to strain relaxation in the Si/SiGe material, the consequential reduction in the interface state density at the gate oxide interface is considered worthwhile.[24]

Samples from ULPCVD material were subjected to the RTA processes shown in Table III, having first undergone two RCA cleans. All annealing was carried out for 20 s in N_2. The anneal temperatures are typical of those used to provide dopant activation for the gate, source and drain regions of MOS devices. A high thermal budget annealing process was carried out at 1050 °C (N_2_high), a low thermal budget annealing process was carried out at 800 °C (N_2_low) and an intermediate thermal budget anneal was performed at 950 °C (N_2_medium).

Control Si grown in the ⟨100⟩ orientation using the Czochralski method was processed and analyzed simultaneously. The Si was uniformly B-doped to 0.5–1.0 Ω cm and micropolished by the supplier (International Wafer Service).

The surface roughness of the samples was analyzed using a Park Scientific Instruments M5 AFM and a Zygo Newview 5000 3D optical surface profiler. The calibration of the

TABLE III. RTA conditions.

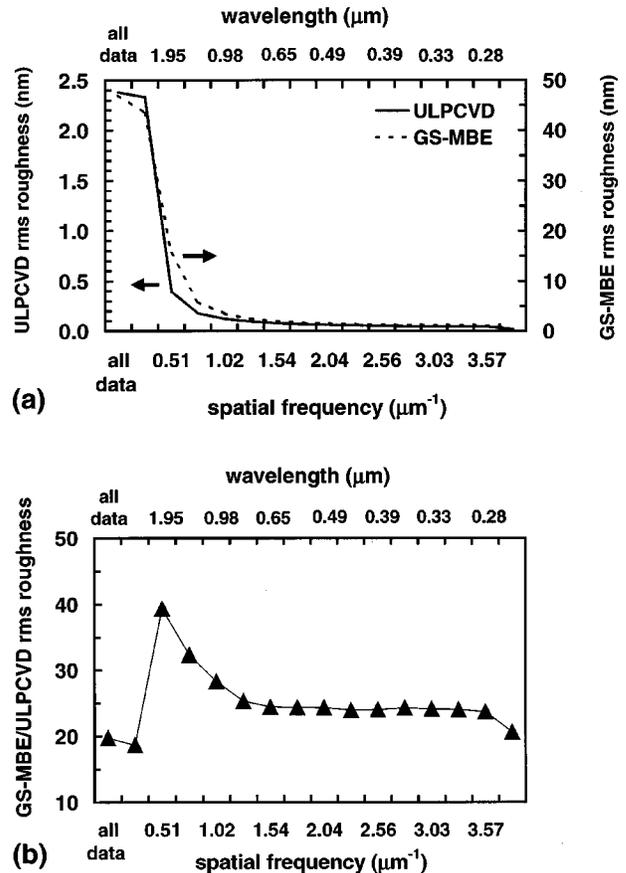| RTA process	Temperature (°C)	Time (sec)	Ambient
N_2_high	1050	20	N_2
N_2_medium	950	20	N_2
N_2_low	850	20	N_2

FIG. 1. Spatial frequency spectra of average rms roughness from all 25 $\times 25$ μm^2 AFM scans of as-grown material: (a) GS-MBE and ULPCVD material, (b) relative roughness of GS-MBE and ULPCVD material.

AFM was performed using an optical grating, and the surface profiler was calibrated using a silicon carbide flat with a roughness less than 0.2 nm as a standard. The vertical resolution was approximately 0.2 and 0.4 nm for the AFM and surface profiler, respectively. For all AFM measurements, several scans around the wafer samples in areas ranging from 1×1 μm^2 to 40×40 μm^2 were obtained in order to study the effects of processing on both large-scale cross-
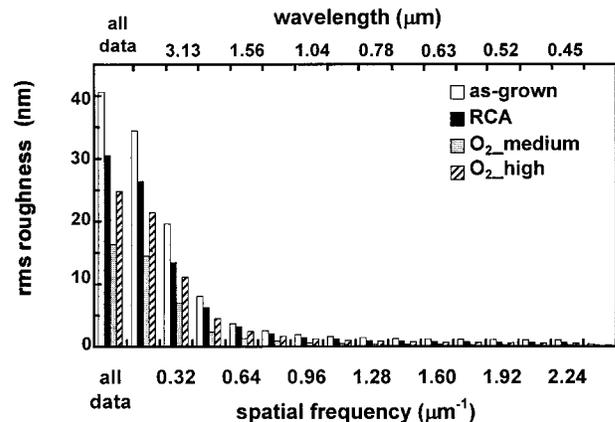

FIG. 2. Spatial frequency plot of average rms roughness from all 40×40 μm^2 AFM scans of as-grown, RCA cleaned and oxidized (O_2_medium and O_2_high) GS-MBE material.

J. Appl. Phys., Vol. 92, No. 3, 1 August 2002
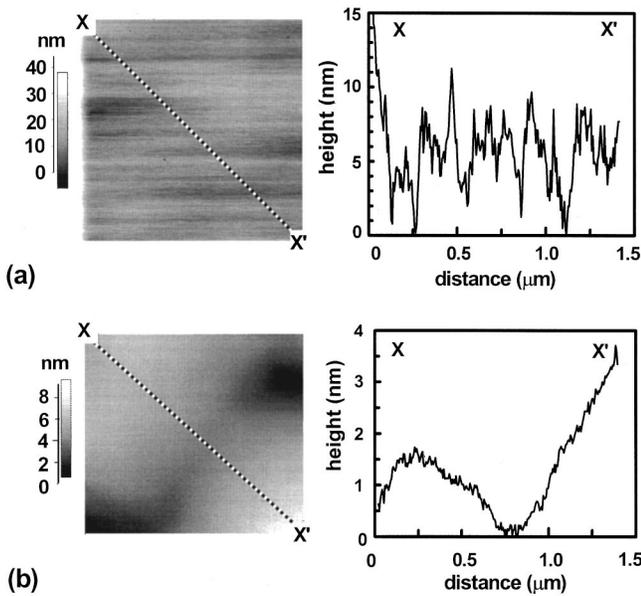
Olsen *et al.*   1301

(a)

(b)

FIG. 3. 1×1 μm^2 AFM images and linescans of strained Si microroughness on cross-hatch peaks of GS-MBE material: (a) as-grown, (b) following RCA cleaning.

III. RESULTS

ULPCVD material was found to display significantly reduced as-grown surface roughness compared with the GS-MBE material. This difference is highlighted in the spatial frequency spectra of the average rms roughness from all the 25×25 μm^2 AFM scans on as-grown GS-MBE and ULPCVD material, shown in Fig. 1(a). The frequency bands were 5% of the total frequency range probed by AFM for 25×25 μm^2 scan areas. Roughness was clearly dominated by the low frequency components, attributed to the characteristic cross-hatching morphology. The average roughness from all scan areas intended to measure cross-hatching was found to be 40 nm on GS-MBE material and 2.5 nm on ULPCVD material. Figure 1(b) shows the roughness of the GS-MBE material relative to ULPCVD material within each frequency band from the 25×25 μm scan areas. The peak in the second lowest frequency band (in the wavelength range 1.95 to 3.90 μm) indicated that the principal cross-hatch period of ULPCVD material is larger than that of GS-MBE material.

The results in Fig. 2 show the effect of processing on the average rms roughness in bands of 5% of the total frequency range probed by AFM from all the 40×40 μm^2 areas measured on the GS-MBE samples. At each frequency band resolved, there was a reduction in roughness following RCA cleaning. The average rms roughness from all the AFM areas analyzed was found to decrease by 30% following cleaning. Moreover, the variation in roughness decreased by over 50% in terms of the standard deviation of the mean value compared with roughness measurements on as-grown material. The ULPCVD material showed a similar trend. The average as-grown rms roughness was reduced by 20% following RCA cleaning, and the variation in roughness was reduced by approximately 60%.

AFM images of typical 1×1 μm^2 areas on as-grown and RCA-cleaned GS-MBE material showed a marked difference

hatching and microroughness on individual cross-hatch periods. The lateral resolution is determined by the sampling frequency of the measurement method. Since the AFM was set up to perform the same number of measurement points in each scan area, smaller scan areas allowed improved lateral resolution suitable for assessing roughness at shorter correlation lengths. Larger scan areas provided more detail on roughness at longer wavelengths, such as cross-hatching. The profiler was only used to study cross-hatching, therefore all scans were 40×40 μm^2. Roughness was assessed in terms of rms values.
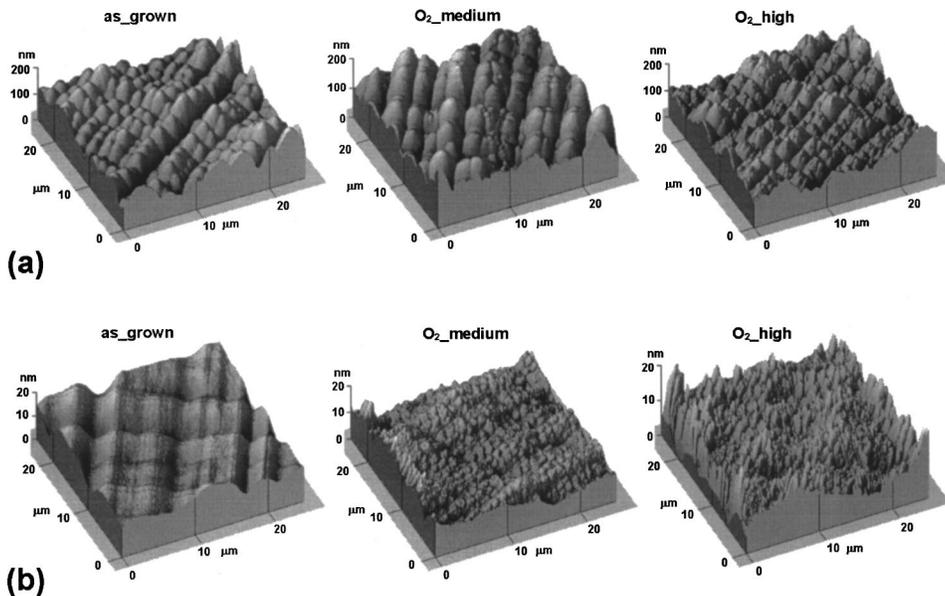

(a)

(b)

FIG. 4. Representative 3D AFM images of 25×25 μm^2 areas on Si/SiGe material indicating the increased roughness following thermal oxidation: (a) GS-MBE samples, (b) ULPCVD samples.
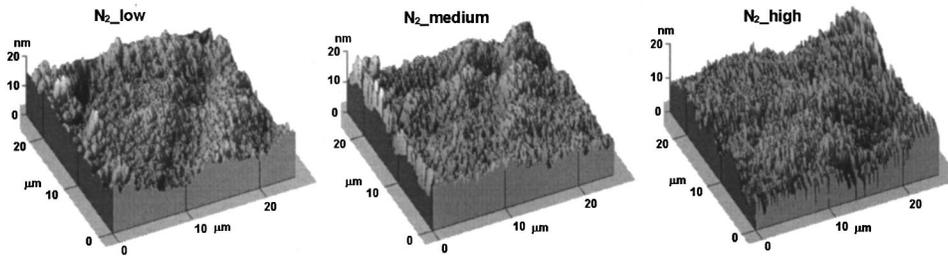
FIG. 5. 25×25 μm^2 3D AFM images of ULPCVD material annealed in N_2.

in surface morphology (Fig. 3). These measurements were taken on cross-hatch peaks and linescans taken across the scan area are also shown. The degraded image quality in Fig. 3(a) is attributed to the intermittent contact of the cantilever tip with the strained Si surface (the AFM was used in contact mode). This can occur if the feedback gain of the AFM is set low; on steep slopes an overshoot can occur as the tip travels up the slope and an undershoot can occur as the tip travels down the slope. If the microroughness is very high, this can lead to streaking of the AFM image, as indicated in Fig. 3(a). No such effects were observed in Fig. 3(b), suggesting a reduction in strained Si microroughness following RCA cleaning, as confirmed by the linescan data. The microroughness of simultaneously processed control Si was found to be below the resolution of the AFM both before and after RCA cleaning. This suggests that the microroughness of strained Si was above that of unstrained Si before and after RCA cleaning.

The effect of oxidation on the average rms roughness of GS-MBE material from 40×40 μm^2 AFM scan areas is shown in Fig. 2. A decrease in roughness following both the 60 min, 800 °C oxidation (O_2_medium) and the 120 min, 800 °C oxidation (O_2_high) is evident. The same trend was observed on 10×10 μm^2 and 25×25 μm^2 scan areas (data not shown). Compared with RCA-cleaned samples, the average reduction in rms roughness was almost 50% following the O_2_medium oxidation and approximately 20% following the O_2_high oxidation. The AFM images revealed the presence of submicron roughening on all areas measured on the GS-MBE sample subjected to the O_2_high oxidation, while only one location investigated on the GS-MBE material following the O_2_medium oxidation displayed such morphology. This led to a greater increase in the variation of roughness data for the GS-MBE sample subjected to the O_2_medium oxidation than for the O_2_high sample. Figure 4(a) shows representative 25×25 μm^2 3D AFM images of the GS-MBE material prior to processing and following the O_2_medium and O_2_high oxidations. The increase in roughness on the O_2_high sample is evident, while the as-grown and O_2_medium samples appear similar. The AFM images of the degraded morphology on the O_2_high sample were

filtered, allowing roughness only at certain frequency bands to be observed, and confirmed that the enhanced microroughness was randomly orientated. The oxidized Si control samples did not display the roughened morphology.

At high temperatures the surface roughness of ULPCVD material was found to degrade to a larger extent than the GS-MBE material. The results in Fig. 4(b) show typical 25×25 μm^2 3D AFM images of ULPCVD surfaces as-grown and following oxidation at 800 °C for 60 min and 120 min (O_2_medium and O_2_high). The overall rms roughness recorded by the AFM did not increase to the high levels observed for GS-MBE material, indicated by the differing scales in Figs. 4(a) and 4(b). However, all oxidations on ULPCVD material, including the lowest thermal budget O_2_low oxidation carried out at 750 °C for 60 min (not shown) displayed a notable increase in surface microroughness. There was little apparent difference in the severity of the microroughness with oxidation condition, contrasting the GS-MBE material and indicating the case with which the ULPCVD material degraded. For the O_2_medium and O_2_high oxidations, the variation in roughness measured around the samples was reduced by approximately 20% from RCA-cleaned values, while only a 2% reduction in the variation in roughness was recorded following the O_2_low oxidation. Further, comparison of Fig. 4(a) with Fig. 4(b) suggests that the roughness at shorter wavelengths following oxidation was more pronounced for the ULPCVD material than for the GS-MBE material. The difference in roughness was observed at wavelengths that could not be quantified from spectral analyses.

The samples of ULPCVD material subjected to RTA were used to investigate whether the enhanced microroughness was caused by high temperature or from the oxidation process itself. The morphology of the annealed samples was found to degrade in the same manner as the oxidized samples of ULPCVD material, as shown in the 25×25 μm^2 3D AFM images in Fig. 5. However, unlike the oxidized samples, roughness correlation lengths appeared to decrease with increasing thermal budget. Overall the roughening of ULPCVD material at shorter correlation lengths was found to be greater following RTA than as a result of oxidation.
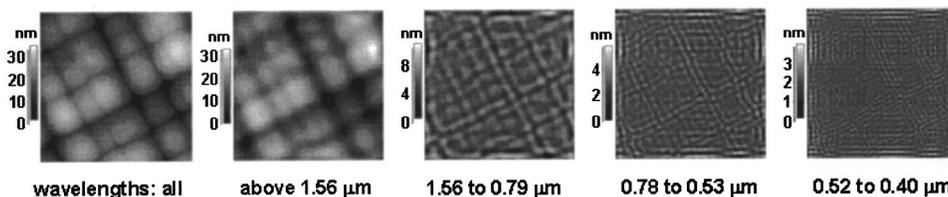

FIG. 6. 10×10 μm^2 AFM images of as-grown GS-MBE material highlighting roughness in the region of the cross-hatch troughs. Roughness at wavelengths other than those in the ranges indicated is filtered from the images.
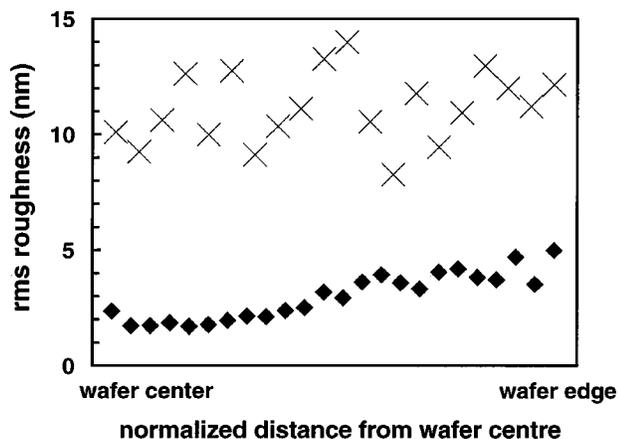
wavelengths: all   above 1.56 μm 1.56 to 0.79 μm 0.78 to 0.53 μm 0.52 to 0.40 μm

FIG. 7. Cross-wafer variation in roughness on GS-MBE and ULPCVD samples oxidized with the O$_2$_high condition (800 °C, 120 min) measured by the optical surface profiler. Measurements on GS-MBE material are denoted by crosses, measurements on ULPCVD material are denoted by diamonds.

In order to examine roughness at specific wavelengths, unfiltered and filtered AFM images were compared, as shown in Fig. 6 for 10×10 μm^2 scans of the same area on as-grown GS-MBE material. The filtered scans mask all roughness wavelengths except those within the range indicated. Figure 6 highlights the presence of roughness along the cross-hatching direction not visible on unfiltered AFM images. The roughness occurred mainly in the regions of the deep troughs, and was visible down to wavelengths of 170 nm on as-grown GS-MBE material and down to 140 nm on RCA-cleaned GS-MBE material. The AFM cantilever scanning effects, observed as vertical and horizontal lines in the higher frequency bands on Fig. 6, ultimately limited detection of such roughness. Enhanced roughness in the troughs of the cross-hatching pattern was observed on as-grown UL-PCVD material down to correlation lengths of 390 nm and there was no change in the minimum correlation length at which the periodic roughness was visible following RCA cleaning.

The cross-wafer variation in roughness was investigated using the optical surface profiler. Although the lateral resolution of the profiler is reduced compared with the AFM due to its lower sampling frequency, the technique is more efficient for obtaining large numbers of measurements and is thus useful for identifying trends. Profiler measurements were therefore performed from the wafer center to wafer edge on the segments of GS-MBE and ULPCVD material subjected to the most aggressive oxidation (O$_2$_high). The results in Fig. 7 indicate that although the radial variation in roughness on the GS-MBE material was negligible, there is a clear deviation of approximately 3 nm in rms roughness between the wafer center and wafer edge on the ULPCVD material. AFM measurements were intentionally performed in locations incorporating both of these regions. Therefore for the ULPCVD material, the range of roughness values observed by AFM is likely to be caused by the radial trend. However, the increased variation in roughness measured by AFM on the GS-MBE material is not a result of any radial trend. The larger dominant cross-hatch period of the UL-

PCVD material led to a closer agreement with roughness measurements carried out using the AFM.

IV. DISCUSSION

Two types of Si/SiGe material with significantly differing as-grown surface roughness have been used to investigate the effect of MOSFET processing on material used for strained Si/SiGe surface channel devices. The results demonstrate that certain processes generally affect all Si/SiGe material, regardless of growth method, whereas other responses appeared to have been more specific to material growth type. Increased surface roughness was observed following high temperature processing steps on both GS-MBE material and ULPCVD material. Despite the reduction in as-grown cross-hatch severity and periodicity of ULPCVD material, the processed material was found to display greater increases in roughness at shorter correlation lengths compared with the GS-MBE material. Oxidation highlighted the differing material growth-dependent reactions of the surface morphology. GS-MBE surface roughness increases with increasing oxidation thermal budget [Figs. 2 and 4(a)], whereas the degradation of ULPCVD material did not appear to be dependent on the oxidation thermal budget [Fig. 4(b)]. Overall the roughness at shorter wavelengths was more marked on thermally oxidized ULPCVD material than on equivalent GS-MBE material. These results contrasted with the nitrogen annealed ULPCVD samples, where the surface morphology degraded with higher annealing temperatures, having enhanced roughness at shorter correlation lengths (Fig. 5). Further, the surface roughness of the thermally processed ULPCVD material appeared to be dominated by shorter correlation lengths compared with those on thermally treated GS-MBE samples (Figs. 4 and 5). Since carrier transport is highly dependent on the roughness correlation length in addition to roughness amplitude, this suggests that superior performance of surface channel HNMOSFET devices cannot be assumed from UL-PCVD material, despite the improved as-grown morphology. The morphological changes which occurred during HNMOSFET processing therefore highlight the need to assess the quality of processed Si/SiGe material rather than as-grown material. In addition, the change in rms roughness values following oxidation and annealing on ULPCVD material were statistically insignificant due to the dominance of the cross-hatching roughness, indicating the inadequacy of relying on roughness measurements alone in analyzing interface morphology.

Roughness wavelength filtering techniques enabled the roughness to be studied at correlation lengths below the dominating low frequency cross-hatching component. The identification of shorter wavelength roughness in the regions of the deep troughs of the cross-hatch pattern established that the roughness was nonuniform over the cross-hatch period (Fig. 6). This roughness was visible down to smaller wavelengths for as-grown GS-MBE material compared with UL-PCVD material. Since cantilever scanning artifacts reduced the resolution of the AFM images, it is likely that the roughness is present at even smaller wavelengths than those detected, such as those affecting carrier transport, providing

further motivation to minimize the cross-hatch severity. The inability to detect the roughness at equivalent correlation lengths on ULPCVD material may be attributed to the reduced cross-hatching roughness compared with GS-MBE material, or from the lower signal to noise ratio on the filtered ULPCVD images. Following RCA cleaning, the orientation-dependent roughness was observed down to slightly shorter wavelengths than on as-grown GS-MBE material. Therefore, while RCA cleaning has been shown to reduce cross-hatching and microroughness, the effect on shorter wavelength roughness along the cross-hatching direction may also be an important factor in the performance and electrical uniformity of HNMOSFET devices. The sample subjected to the 800 °C oxidation for 60 min (O₂_medium) did not display any change in the correlation length of roughness in the regions of the deep troughs, and high levels of randomly oriented microroughness on the GS-MBE material oxidized at 800 °C for 120 min (O₂_high), and all thermally treated ULPCVD samples prevented detection of such roughness on these samples. The importance of filtering techniques in assessing Si/SiGe material quality has thus been highlighted since the roughness is not apparent using conventional AFM imaging.

The present finding that improved strained Si surface roughness in terms of both the dominant cross-hatching and microroughness on cross-hatch peaks following RCA cleaning contrasts Czochralski Si, where an increase in microroughness with similar RCA cleaning has been reported.[23,25,26] The increase in microroughness on unstrained Si is considered to originate from point defects.[23,26] It is likely that a higher defect density on strained Si causes the increased microroughness of strained Si compared with Czochralski Si. Minimizing the defect density in addition to optimizing the RCA cleaning procedure may assist in reducing the strained Si microroughness further, including that along the cross-hatching direction. Reducing the NH₄OH concentration has been found to minimize surface roughness while yielding a negligible impact on the electrical oxide quality of unstrained Si.[23,27] Such adjustments could prove particularly valuable since the roughness correlation length at which the roughness reaches a constant value has been shown to increase with prolonged RCA1 cleaning.[28] Indeed, for Si/SiGe structures the amount of material removed during cleaning must be considered in the epitaxial layer design. Modifications to the DI rinse carried out between RCA1 and RCA2 may also assist in reducing the surface microroughness.[23]

It has been reported that SiGe is removed preferentially compared with Si during RCA cleaning.[29,30] This is thought to arise from the chemical bonds at surface defect sites being weaker than those of perfect bond sites, and the association of higher defect concentrations with higher Ge ratios in SiGe.[30] Rapid etching of Ge atoms present on an upper surface layer has additionally been identified as an explanation for the enhanced reaction rate during RCA cleaning.[30] On the account that cross-hatching reduces following RCA cleaning, this suggests that an increase in the segregated Ge concentration is present on the cross-hatch peaks of Si/SiGe mate-

rial. Further, the RCA etch rate may be dependent on strain, which varies across the cross-hatch period.

The results presented above indicate that the effect of oxidizing strained Si contrasts with unstrained Si, which smoothes after an initial roughening stage.[31–34] Several factors have been proposed that may influence the Si/SiO₂ interface roughness of unstrained Si, including the crystallographic orientation of the Si surface, local stress at the Si/SiO₂ interface, wafer polishing methods, and defect density, in addition to the precise oxidation and pre-oxidation cleaning conditions.[31,33,35] These factors are also likely to influence the surface roughness of strained Si following oxidation. Furthermore, the effects of oxidation on interface roughening have been found to be particularly prominent on rough start material.[31,33]

Local regions of stress at Si/SiO₂ interface irregularities may also cause roughness. Thermal oxide is compressively strained, whereas Si is under tensile strain at the Si/SiO₂ interface. For dry oxidation, viscous flow is at 950–1000 °C.[33] If the oxide growth temperature exceeds the viscous flow temperature, continuous stress relief occurs during oxidation. However, the oxidations carried out in the present study were below the point of viscous flow, therefore there is no viscous flow and no interfacial stress relief at surface irregularities. The presence of strain at interface irregularities such as defects causes fluctuating oxidation reaction rates and consequently Si/SiO₂ interface roughness. Since the Si/SiGe start material in the current study is intentionally strained and displays enhanced microroughness compared with unstrained material, the oxidation rates and thus the final interface roughness is likely to vary to a greater extent than on unstrained Si, as observed. On a larger scale, it is possible that variation in strain across the cross-hatch period could give rise to a variation in oxidation along the cross-hatch period.

Decomposition of surface oxide when wafers are heated to high temperatures in low partial pressures can also cause Si/SiO₂ interface roughness. The oxide is removed by a Si/SiO₂ reaction that produces volatile SiO which can etch the Si surface.[35] It has been proposed that defect sites in unstrained Si cause decomposition of thin oxides by the defects acting as nucleation centers.[33] The degradation of strained Si even for relatively long oxidation periods again may be attributed to a high defect density of strained Si. Further, the ease at which the ULPCVD material degraded in the present experiments compared with the GS-MBE material may be indicative of a higher defect density in ULPCVD material. Alternatively, a lower oxidation rate of strained Si compared with unstrained Si could result in oxide growth being unable to pass the initial linear oxidation stage associated with enhanced roughness.

Wet and plasma oxidation of SiGe have been reported to occur at a faster rate than Si.[36–39] Although dry oxidation may have different mechanisms governing the growth of thin oxides of SiGe,[40] the increase in strained Si microroughness following oxidation may have originated from Ge clusters present in the Si surface layer as a result of segregation. Therefore contrary to conventional Si CMOS, reduced thermal budget oxidations commensurate with device scaling

strategies may assist in minimizing the effect of interface scattering in strained Si/SiGe surface channel HNMOSFETs.

The increase in ULPCVD material surface roughness at short correlation lengths after annealing in N_2 is important and demonstrates that the surface morphology of strained Si is primarily affected by thermal budget as opposed to ambient. The roughening of the Si/SiGe material during high temperature processes could be a consequence of the Ge ions reorganizing towards a minimum surface energy configuration at temperatures not experienced by material grown at such low temperatures, as used here. The reorganization of Ge at high thermal budgets is also likely to be highly relevant for high temperature inert annealing stages, and agrees with the similarity between the roughening observed in N_2 and O_2 ambients presented above.

While severe degradation to both types of Si/SiGe material were evident as a result of thermal processing, the improved strained Si morphology following low temperature RCA cleaning was notable. Since high temperature processing is not required for MODFET fabrication, no increase in the surface roughness of Si/SiGe MODFET structures is anticipated. Thus the ability to maintain the Si/SiGe morphology following MODFET device processing could be a key factor in the successful performance of Si/SiGe MODFETs.

Oxidation and annealing induced surface roughening on strained Si will additionally influence the quality of silicides formed on the source and drain regions. In order to achieve extrinsic as well as intrinsic performance gains in surface channel HNMOSFET devices, it is likely that higher temperature material growth, which has to date lead to the most promising strained Si/SiGe HNMOSFET performance[8] or use of chemical mechanical polishing (CMP) on the SiGe VS[13,41] may be beneficial. Since surface channel HNMOSFET devices require only enough strain to split the conduction bands, it is anticipated that reducing the alloy composition to a much lower Ge content (e.g., ~15%) could yield improved device performance arising from enhanced material properties without the difficulties relating to high temperature processing of high alloy composition material.

V. SUMMARY

The GS-MBE and ULPCVD material in the present study were found to exhibit the characteristic cross-hatching pattern associated with relaxed SiGe alloys. CVD material displayed vastly improved as-grown morphology compared with MBE material, but was found to be more susceptible to increased surface microroughness from high thermal budget processing than MBE material, suggesting that it is unsuitable to use unprocessed Si/SiGe material quality in terms of cross-hatching roughness as an indicator for strained Si/SiGe MOSFET device performance. The increase in strained Si surface roughness at small lateral length scales resulted from high thermal budget processing in both O_2 and N_2 ambients. Low temperature RCA cleaning was found to significantly reduce both the cross-hatching roughness and the large cross-wafer variation in roughness on CVD and MBE Si/SiGe material, in addition to lowering the microroughness of GS-MBE strained Si material.

Roughening measurements on strained Si/SiGe material were found to be sensitive to sampling frequency and identification of small-scale roughness along the deep cross-hatch troughs required AFM image filtering. A small increase in cross-hatching was observed towards the wafer edge on the CVD material, whereas no radial trend in roughness could be detected on MBE material.

The closer agreement between experimental $I-V$ data for strained Si/SiGe n-channel MODFETs and theory compared with strained Si/SiGe n-channel MOSFETs is considered to be due to the differences in the fabrication process; since MODFETs do not require high temperature processing, such devices avoid increased surface roughness. Reducing the alloy composition, CMP, lower thermal budget MOS processing and increasing the material growth temperature may promote robustness of strained Si/SiGe material during fabrication, yielding greater performance advantages of surface channel HNMOSFET devices.

[1] D. J. Paul, Thin Solid Films **321**, 172 (1998).

[2] B. S. Meyerson, IBM J. Res. Dev. **44**, 391 (2000).

[3] R. People, IEEE J. Quantum Electron. **QE-22**, 1696 (1986).

[4] A. G. O'Neill and D. A. Antoniadis, IEEE Trans. Electron Devices **43**, 911 (1996).

[5] *2001 International Technology Roadmap for Semiconductors*, internet address: http://public.itrs.net

[6] K. Ismail, S. Rishton, J. O. Chu, K. Chan, and B. S. Meyerson, IEEE Electron Device Lett. **14**, 348 (1993).

[7] A. G. O'Neill, P. Routley, P. K. Gurry, P. A. Clifton, H. Kemhadjian, J. Fernandez, A. G. Cullis, and A. Benedetti, Semicond. Sci. Technol. **14**, 784 (1999).

[8] K. Rim, S. Koester, M. Hargrove, J. Chu, P. M. Mooney, J. Ott, T. Kanarsky, P. Ronsheim, M. Ieong, A. Grill, and H.-S. Wong, Symposium on VLSI Technology, p. 59 (2001).

[9] J. Koga, S. Takagi, and A. Toriumi, Tech. Dig. - Int. Electron Devices Meet. **1994**, 475.

[10] T. Ohmi, K. Kotani, A. Teramoto, and M. Miyashita, IEEE Electron Device Lett. **12**, 652 (1991).

[11] A. G. Sabnis and J. T. Clemens, Tech. Dig. - Int. Electron Devices Meet. **1979**, 18.

[12] S. Badcock and A. O'Neill, Superlattices Microstruct. **28**, 363 (2000).

[13] N. Sugii, D. Hisamoto, K. Washio, N. Yokoyama, and S. Kimura, Tech. Dig. - Int. Electron Devices Meet. **2001**, 737.

[14] T. Yamanaka, S. J. Fang, H. Lin, J. P. Snyder, and C. R. Helms, IEEE Electron Device Lett. **17**, 178 (1996).

[15] A. Pirovano, A. L. Lacaita, G. Ghidini, and G. Tallarida, IEEE Electron Device Lett. **21**, 34 (2000).

[16] J. W. P. Hsu, E. A. Fitzgerald, Y. H. Xie, P. J. Silverman, and M. J. Cardillo, Appl. Phys. Lett. **61**, 1293 (1992).

[17] S. Y. Shiryaev, F. Jensen, and J. W. Petersen, Appl. Phys. Lett. **64**, 3305 (1994).

[18] Y.-H. Xie, E. A. Fitzgerald, D. Monroe, G. P. Watson, and P. J. Silverman, Jpn. J. Appl. Phys. **33**, 2372 (1994).

[19] Z. Kovats, T. Salditt, T. H. Metzger, J. Peisl, T. Stimpel, H. Lorenz, and K. Ismail, J. Phys. D **32**, 359 (1999).

[20] N. J. Woods, G. Breton, H. Graoui, and J. Zhang, J. Cryst. Growth **227**, 735 (2001).

[21] J. M. Hartmann, B. Gallas, R. Ferguson, J. Fernandez, J. Zhang, and J. J. Harris, Semicond. Sci. Technol. **15**, 362 (2000).

[22] J. W. Matthews and A. E. Blakeslee, J. Cryst. Growth **27**, 118 (1974).

[23] T. Ohmi, M. Miyashita, M. Itano, T. Imaoka, and I. Kawanabe, IEEE Trans. Electron Devices **39**, 537 (1992).

[24] S. Wolf and R. N. Tauber, *Silicon Processing for the VLSI Era Volume 1: Process Technology* (Lattice, Sunset Beach, CA, 1986).

[25] H. Mishima, T. Yasui, T. Mizuniwa, M. Abe, and T. Ohmi, IEEE Trans. Semicond. Manuf. **2**, 69 (1989).

[26] M. Miyashita, T. Tusga, K. Makihara, and T. Ohmi, J. Electrochem. Soc. **139**, 2133 (1992).

[27] T. Couteau, M. McBride, D. Riley, and P. Peavey, Semiconductor International Web Site, internet address: http://www.semiconductor.net

[28] M. Gotoh, K. Sudoh, and H. Iwasaki, J. Vac. Sci. Technol. B **18**, 2165 (2000).

[29] F. S. Johnson, D. S. Miles, D. T. Grider, and J. J. Wortman, J. Electron. Mater. **21**, 805 (1992).

[30] K. Koyama, M. Hiroi, T. Tatsumi, and H. Hirayama, Appl. Phys. Lett. **57**, 2202 (1990).

[31] J. Koga, S. Takagi, and A. Toriumi, Jpn. J. Appl. Phys. **35**, 1440 (1996).

[32] M. Niwa, M. Udagawa, and K. Okada, Appl. Phys. Lett. **63**, 675 (1993).

[33] S. J. Fang, W. Chen, T. Yamanaka, and C. R. Helms, J. Electrochem. Soc. **144**, 2886 (1997).

[34] H. C. Lu, E. P. Gusev, E. Garfunkel, and T. Gustafsson, Surf. Sci. **351**, 111 (1996).

[35] C. J. Solfield and A. M. Stoneham, Semicond. Sci. Technol. **10**, 215 (1995).

[36] F. K. LeGoues, R. Rosenberg, T. Nguyen, F. Himpsel, and B. S. Meyerson, J. Appl. Phys. **65**, 1724 (1989).

[37] L. S. Riley and S. Hall, J. Appl. Phys. **85**, 6828 (1999).

[38] N. Nayak, K. Kamjoo, J. S. Park, J. C. S. Woo, and K. L. Wang, Appl. Phys. Lett. **57**, 369 (1990).

[39] J. P. Zhang, P. L. F. Hemment, and E. H. C. Parker, Semicond. Sci. Technol. **14**, 484 (1999).

[40] N. Nayak, K. Kamjoo, J. C. S. Woo, J. S. Park, and K. L. Wang, Appl. Phys. Lett. **56**, 66 (1990).

[41] M. T. Currie, S. B. Samavedam, T. A. Langdo, C. W. Leitz, and E. A. Fitzgerald, Appl. Phys. Lett. **72**, 1718 (1998).