Study of Single- and Dual-Channel Designs for High-Performance Strained-Si–SiGe n-MOSFETs

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***Abstract*—Results comparing strained-Si–SiGe n-channel MOSFET performance of single-and dual-surface channel devices fabricated using 15% Ge content SiGe virtual substrates are presented. Device fabrication used high thermal budget processes and virtual substrates were not polished. Mobility enhancement factors exceeding 1.6 are demonstrated for both single-and dual-channel device architectures compared with bulk-Si control devices. Single-channel devices exhibit improved gate oxide quality, and larger mobility enhancements, at higher vertical effective fields compared with the dual-channel strain-compensated devices. The compromised performance enhancements of the dual-channel devices are attributed to greater interface roughness and increased Ge diffusion resulting from the $Si_{0.7}Ge_{0.3}$ buried channel layer.**

***Index Terms*—Dual-channel, gate oxide interface, interface roughness, mobility enhancement, n-MOSFETs, silicon–germanium, single-channel, strained-silicon, thermal budget, virtual substrate.**

I. Introduction

THE 4.2% difference in the lattice constants of Si and Ge atoms can be used to create high-mobility strain-engineered devices. Electron mobility is enhanced in strained-Si compared with bulk-Si due to tensile strain splitting the six-fold degenerate conduction band valleys and causing the resulting two-fold band with lower energy and reduced in-plane effective mass to be preferentially filled [1]. A four-fold band with increased energy is also created, which additionally contributes to the higher electron mobility through a reduction in intervalley scattering. Tensile strained-Si layers are, thus, useful for electron channels of high mobility n-MOSFETs. Epitaxial growth of Si on relaxed SiGe alloys creates such strained-Si layers due to the larger atomic spacing of Ge, and consequently relaxed SiGe alloys [2], compared with Si. Hole transport is improved in both tensile strained-Si and compressively strained-SiGe compared with bulk-Si. Modifications to the electronic band structure and a reduction of the hole effective mass have been found to increase mobility in strained-SiGe by five times [3]. Epitaxial growth of SiGe on either bulk-Si or relaxed SiGe alloys with a lower Ge content than the growing film can produce compressively strained-SiGe.

There are some challenges in using strain to enhance the performance of CMOS devices and many of these are related to the critical thickness of a strained-layer [4]. If a strained-layer is grown above the critical thickness, strain relaxes with the introduction of misfit defects at the strained-Si–SiGe heterointerface and the enhanced transport properties arising from the strain are lost. Minimizing the exposure of the strained-material to high thermal budgets during processing reduces the probability of material degradation, since high temperatures cause strain to relax. However, non-optimized processing conditions may lead to degraded extrinsic performance [5]–[7]. Reducing the thickness of the strained-layer may protect the material against strain relaxation, but very thin channel layers compromise the performance gains achievable [8]. Dual-channel structures [9] minimize the cumulative strain within the devices by the sequential growth of tensile and compressively strained-layers, thereby allowing higher thermal budgets to be used before the onset of strain relaxation. The strain-compensation within the dual-channel structure can alternatively be traded off against thicker strained-channel layers. By growing a compressive strained-SiGe layer followed by a tensile strained-Si layer on a single-relaxed SiGe "virtual substrate," the band offsets between the oppositely strained-materials can be used to create high mobility surface n- and buried p-channel MOSFETs. This dual-channel CMOS architecture has been shown theoretically to maximize the transconductance of both n- and p-channel devices for a range of achievable mobilities [10].

The benefits of using dual-channel device architectures have recently received attention [3], [9]–[13]. Rim *et al.* have investigated p-channel performance in dual-channel architectures using a compressively strained-SiGe layer below a tensile strained-Si layer [11], but have only provided a limited assessment of electron mobility in such structures. Researchers at the Massachusetts Institute of Technology (MIT) have considered dual-channel structures with a view to optimizing buried p-MOS devices using relaxed $Si_{1-x}Ge_x$ virtual substrates (VS), with $0.3 < x < 1$ [3], [12], [13], concluding that surface electron mobility is not influenced by the presence of a compressive SiGe buried p-channel layer. However, the devices had long channel lengths and were fabricated using a low thermal budget process, unlike conventional CMOS. Optimizing the VS for n-channel performance is paramount, since n-MOSFETs often dominate circuit speed. We have previously reported strained-Si n-channel MOSFETs fabricated using a high thermal budget on a dual-channel architecture, which was designed for obtaining

Manuscript received October 15, 2003; revised February 18, 2004. This work was supported by the Engineering and Physical Sciences Research Council, U.K. The review of this paper was arranged by Editor C.-Y. Lu.

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Digital Object Identifier 10.1109/TED.2004.830652

high n-channel performance [9]. The devices were fabricated on ultrahigh vacuum chemical vapor deposition (CVD) virtual substrate material and demonstrated some of the highest performance gains reported to date compared with unstrained-Si control devices over a wide range of gate lengths. However, the primary aim of incorporating the buried strained-SiGe layer is to improve p-channel devices; in order for the increased complexity of dual-channel designs to be worthwhile, n-channel performance must not be compromised compared with devices having single-strained-Si surface channels, which benefit from having less complicated layer structures and processing requirements. At present, there are a number of uncertainties in understanding the advantages to strained-Si n-channel devices by using a dual-channel structure, and thus far, an experimental investigation has not been undertaken. Improved performance may be anticipated due to the increased confinement of electrons in the high mobility strained-Si surface channel compared with single-channel strained-Si MOSFETs. However, increased Ge diffusion into the tensile strained-Si channel from the high Ge-content strained-SiGe layer during processing, and additional complexity in the material growth, may offset any advantages offered by the double quantum well structure. In this paper, we report the first comparative study of single-and dual-channel strained-Si n-MOSFET devices fabricated together on virtual substrate alloy compositions suitable for high performance n-channel MOSFETs. The devices were processed using a high thermal budget. In Section II the device designs and fabrication process are described. The n-MOSFETs comprised of a strained-Si surface channel grown on either a compressively strained-SiGe layer or a relaxed SiGe virtual substrate using ultralow pressure CVD. The impact of layer architecture on strained-Si MOSFET operation and manufacturability are discussed in Section III. Significant performance gains are presented for the strained-Si–SiGe devices compared with conventional unstrained-devices. Section IV provides a summary of the main conclusions of the work.

II. Epitaxial Growth and Device Fabrication

Strained-Si n-channel MOSFETs were fabricated on relaxed $Si_{0.85}Ge_{0.15}$ virtual substrates (VS). The VS were grown by ultralow-pressure CVD (ULPCVD) in a modified molecular-beam epitaxy (MBE) system [14] using a grading rate of 10% Ge/μm. The VS growth temperature was 650 °C. single-and dual-channel layer structures are shown in Fig. 1(a) and 1(b), respectively. For the single-channel devices, a 16-nm strained-Si layer was grown on the VS, which resulted in a final strained-Si channel thickness of approximately 5 nm due to surface cleans and gate oxidation, as determined by transmission electron microscopy (TEM) on fully processed devices. The as-grown VS alloy composition, layer thickness and strain were verified by secondary ion mass spectrometry (SIMS), TEM and X-ray diffraction (XRD). The threading dislocation density was found to be approximately 1×10^5 cm^{-2} using a Secco etch solution consisting of 0.15 M $K_2Cr_2O_7$: HF : $H_20 = 1 : 2 : 30$. The root mean square (RMS) surface roughness of a strained-Si layer grown directly

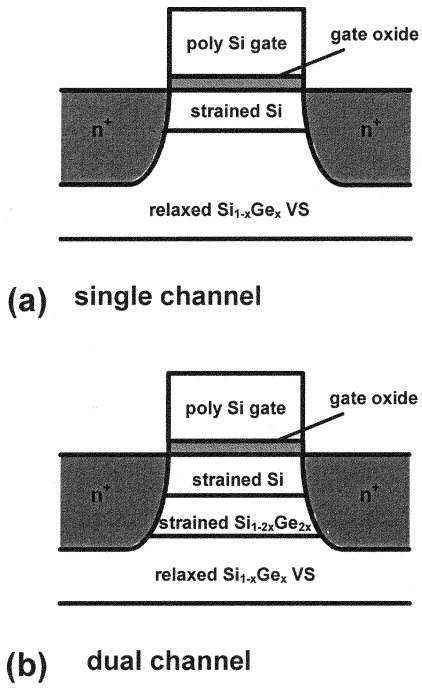

Fig. 1. Single- and dual-channel layer architectures. (a) Single-channel and (b) dual-channel.

on a 20% VS at the same time as the device wafers was measured as 5 nm on 20 μm $\times$ 20 μm scans using atomic force microscopy (AFM) at several locations around the wafer. Since the RMS roughness increases with increasing Ge content in the VS for this growth system [15], 5 nm represents the upper limit of as-grown surface roughness for the $Si_{0.85}Ge_{0.15}$ VS used for device fabrication in the current work. SiGe alloy compositions on fully processed devices were confirmed by SIMS and electron dispersive spectroscopy. Dual-channel architectures were also grown on a $Si_{0.85}Ge_{0.15}$ VS. A compressively strained-12 nm $Si_{0.70}Ge_{0.30}$ layer was grown between the strained-Si surface channel and the $Si_{0.85}Ge_{0.15}$ VS. In both device architectures, the channel layers were grown at reduced temperature (550 °C) in order to minimize Ge segregation into the channel. Fig. 2 illustrates the energy bands for the single-and dual-channel device architectures under inversion conditions for p- and n-channel devices. Both structures have band alignments, which yield surface n-channel devices. However, the valence band offset is significantly larger between the strained-Si and the compressively strained-$Si_{0.70}Ge_{0.30}$ layer in the dual-channel structure than between the strained-Si and $Si_{0.85}Ge_{0.15}$ in the single-channel device. Therefore, only the dual-channel structure can offer high mobility buried p-channel operation. Although hole mobility is enhanced in both tensile strained-Si and compressively strained-SiGe, simulations which assume ideal processing conditions and a negligible effect of Ge diffusion into the strained-Si have shown that higher p-MOS transconductance is achieved from the dual-channel device compared with a surface p-MOS device [10]. Transconductance decreases in a buried channel architecture due to increased separation between the gate and the buried channel, whereas transconductance decreases in a surface channel device

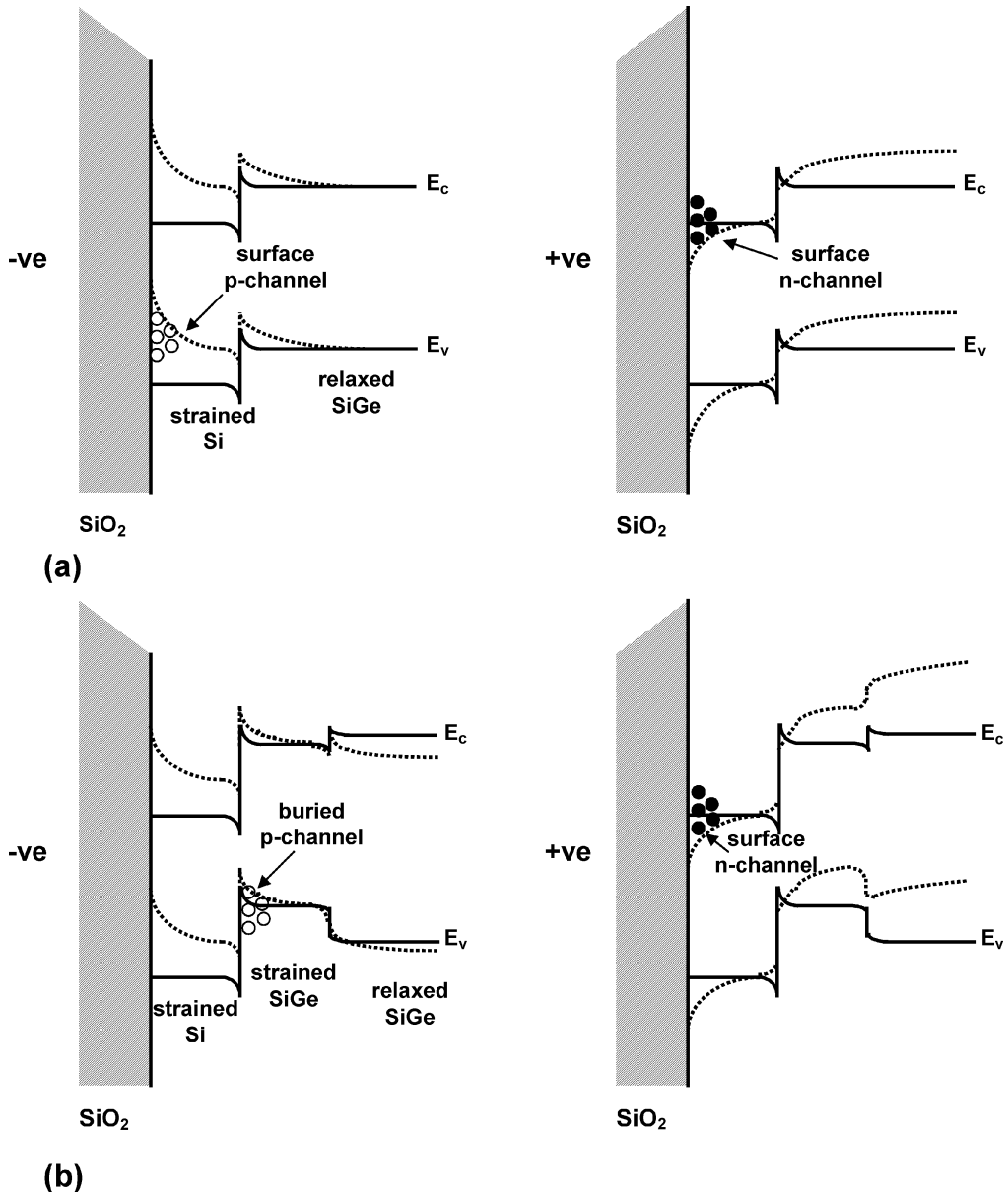

Fig. 2. Energy band diagrams showing carrier confinement in inversion for n- and p-MOSFETs fabricated on a (a) single-channel architecture and (b) dual-channel architecture.

due to reduced mobility arising from increased surface roughness scattering. The optimum layer architecture for maximum transconductance is determined by both the gate to channel separation and the achievable mobility. For the most likely range of mobilities achievable, a hole channel buried between 2 and 4 nm below the gate oxide interface is predicted to yield the highest values of transconductance [10].

In order to investigate the impact of Ge diffusion on oxide quality, single-channel n-MOSFETs were also fabricated on a $Si_{0.70}Ge_{0.30}$ VS. This enabled a comparison of the single-channel strained-Si–$Si_{0.70}Ge_{0.30}$ devices with dual-channel structures, where a compressive $Si_{0.70}Ge_{0.30}$ layer was set back from the oxide by the same strained-Si thickness as the single-channel device.

Strained-Si–SiGe device fabrication followed a 0.25-μm CMOS process. Oxide was deposited and active areas were defined by wet etching using buffered hydrogen fluoride (HF). Thermal oxidation at 800 °C for 1 h produced a 6-nm gate oxide (measured by TEM on fully processed devices). Annealing in nitrogen was subsequently carried out for 15 min at 800 °C in order to reduce the gate oxide interface trap density. Polysilicon was deposited for the gate electrode, implanted with P, and annealed at 800 °C for 30 min. Devices with a range of gate lengths were patterned using electron-beam lithography. An additional thermal oxidation at 800 °C was carried out prior to the source/drain implants in order to protect the strained-Si surface. As and P were used for the source, drain, and gate dopants and were annealed at 1050 °C for 20 s. Silox and BPSG were deposited for the interlayer dielectric materials and contact vias were etched and filled with a Ti–TiN liner and Al metallization.

Si control devices were processed simultaneously on bulk Czochralski wafers and received implanted well doping using B. The SiGe wafers were *in situ* doped with a background

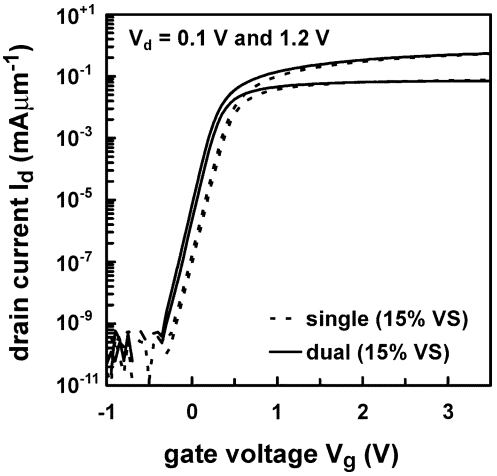

Fig. 3. Log drain current (I_d) versus gate voltage (V_g) for 0.3-μm gate length strained-Si–SiGe MOSFETs fabricated on a $Si_{0.85}Ge_{0.15}$ virtual substrate. The single-channel device exhibits improved DIBL compared with the dual-channel device, and both device architectures demonstrate excellent subthreshold slopes and on/off-state I_d characteristics. Measurements were carried out using a drain voltage (V_d) of 0.1 and 1.2 V.

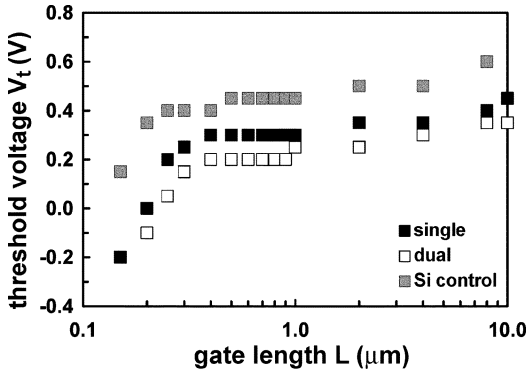

Fig. 4. Threshold voltage (V_t) rolloff for the single-channel, dual-channel, and Si control devices.

doping of B to a concentration of $\sim 5 \times 10^{17}$ cm^{-3} (determined by SIMS). The retrograde doping was set back from the strained-Si channel by approximately 75 nm in the $Si_{0.85}Ge_{0.15}$ VS. Process simulations carried out using Silvaco software [16] and using B diffusivities taken from the literature [17], [18] determined that an initial set back layer thickness of 75 nm would result in approximately 50 nm of undoped $Si_{0.85}Ge_{0.15}$ between the 5×10^{17} cm^{-3} B diffusion edge, and the channel layers after processing. The single-channel strained-Si–$Si_{0.70}Ge_{0.30}$ devices were grown identically to the $Si_{0.85}Ge_{0.15}$ VS devices, although the initial doping set back layer thickness was reduced to 62 nm in the $Si_{0.70}Ge_{0.30}$ VS to compensate for the lower diffusivity of B in $Si_{0.70}Ge_{0.30}$ compared with B in $Si_{0.85}Ge_{0.15}$.

III. Results and Discussion

The benefits of dual-channel architectures arise from the high Ge-content strained-layer above the relaxed $Si_{1-x}Ge_x$ VS providing improved p-channel performance, material stability, and design flexibility [10], [19]. However, the impact on device performance of a high thermal budget, as encountered in a CMOS process, combined with the high Ge-content layer, as found in the dual-channel architecture, has not been experimentally investigated for strained-Si–SiGe n-MOSFETs on a $Si_{0.85}Ge_{0.15}$ VS. A comparison of single-and dual-channel device performance was undertaken using n-MOSFETs with the same surface channel strain. Subthreshold characteristics for the best performing single-and dual-channel devices fabricated on $Si_{0.85}Ge_{0.15}$ virtual substrates are illustrated in Fig. 3. The devices have 0.3-μm gate lengths and were measured at a drain voltage (V_d) of 0.1 and 1.2 V. The subthreshold slopes of both strained-Si–SiGe devices were found to be approximately 90 mV/dec and equivalent to the Si control devices. The dual-channel devices exhibited lower threshold voltages (V_t) than the single-channel devices, due to the band alignment and increased oxide trap density. However, V_t roll-off was similar for all device architectures (Fig. 4). The threshold voltage was defined as the gate voltage (V_g) where $I_d = 70$ nA/μm at $V_d = 0.1$ V. The electrostatic integrity of the devices was assessed in terms of drain-induced barrier lowering (DIBL) and was found to be improved in the single-channel device compared with the dual-channel devices. DIBL can be affected by gate oxide quality and was found to be 20 mV/V for the single-channel device and 60 mV/V for the dual-channel device. However, both sets of strained-Si devices were grown with the same set back layer thickness between the B doping in the $Si_{0.85}Ge_{0.15}$ VS, and the strained-Si surface channel (75 nm). Thus, retarded diffusion of B in the compressively strained-$Si_{0.70}Ge_{0.30}$ layer may have led to a slightly higher channel doping in the single-channel device than in the dual-channel device, contributing to the lower values of DIBL obtained from the single-channel devices. Nevertheless, the standard deviation of the mean value of DIBL measured on all 0.3 μm gate length devices across the wafers was found to be three times as large for the dual-channel devices as it was for the single-channel devices.

The field-effect mobility (μ_{fe}) is presented as a function of vertical effective field (E_{eff}) in Fig. 5(a) for representative 10 μm gate length single-and dual-channel n-MOSFETs fabricated on $Si_{0.85}Ge_{0.15}$ VS. Si control data are also shown. The measurements were carried out at $V_d = 0.1$ V. While both strained-Si–SiGe devices exhibit significantly enhanced performance compared with the Si control device, the single-channel device achieves a higher mobility than the dual-channel device over the whole E_{eff} range investigated. At $E_{\text{eff}} = 0.4$ MVcm^{-1}, the mobilities are 520, 495, and 305 cm^{2}V^{-1}s^{-1} for the single, dual, and Si control devices, respectively. The peak mobility demonstrated by the dual-channel devices fabricated on ULPCVD material does not match that demonstrated by our previous strained-Si–SiGe dual-channel devices fabricated using an identical process on ultrahigh vacuum CVD material (UHV-CVD) [9]. Detailed material analysis has recently suggested that the ULPCVD growth conditions used for device fabrication in this paper led to degraded SiGe virtual substrate quality compared with SiGe virtual substrates grown at higher temperature [20]. Therefore, the electrical performance of both the single-and dual-channel devices presented in the current work may be enhanced further through fabrication on optimized material.

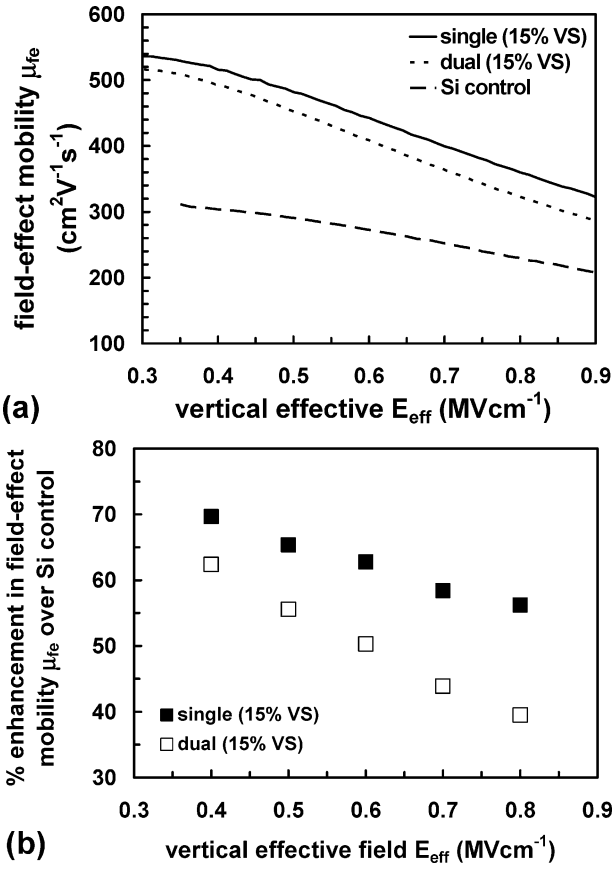

Fig. 5. Comparison of field-effect mobility ($\mu_{\rm fe}$) in single, dual, and Si control devices measured on 10-μm gate length devices at a drain voltage (V_d) = 0.1 V (strained-Si–SiGe devices fabricated on a $Si_{0.85}Ge_{0.15}$ virtual substrate). (a) $\mu_{\rm fe}$ versus vertical effective field ($E_{\rm eff}$). (b) Enhancement in $\mu_{\rm fe}$ over Si control for single-and dual-channel devices.

Fig. 5(b) shows the mobility enhancement of the single-and dual-channel devices compared with the Si control as a function of vertical effective field. The divisor is the bulk-Si reference mobility at each value of field. At room temperature, carrier transport is dominated by Coulomb, phonon, and surface roughness scattering at low, medium, and high vertical effective fields, respectively [21]. Fig. 5(b) illustrates that at low $E_{\rm eff}(\sim 0.4\,{\rm MVcm}^{-1})$, the single-channel device exhibits a mobility enhancement of approximately 70% compared with the Si control whereas the mobility enhancement for the dual-channel device is slightly lower (∼62%). However, at higher fields the difference in mobility enhancement between the two strained-Si–SiGe devices compared with bulk-Si increases significantly. At $E_{\rm eff} = 0.8\ {\rm MVcm}^{-1}$, the enhancement is found to be approximately 55% for the single-channel device, and 40% for the dual-channel device. The higher mobility of the single-channel device at high $E_{\rm eff}$ is particularly important for short-channel devices, which operate at higher $E_{\rm eff}$ due to increased substrate doping required to suppress short channel effects. These results therefore demonstrate that strained-Si–SiGe is a viable solution for obtaining high performance scaled devices. The higher mobility may alternatively be used to attain high performance devices without the retooling costs associated with conventional geometric scaling, or equal current drive at a reduced voltage for low power integrated circuits.

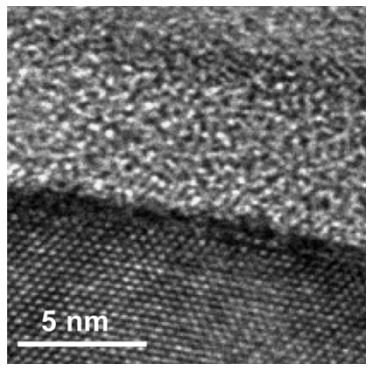

Fig. 6. High-resolution TEM image of the strained-Si/gate oxide interface on a strained-Si–$Si_{0.70}Ge_{0.30}/Si_{0.85}Ge_{0.15}$ dual-channel device.

Previous work has reported a maximum electron mobility enhancement of approximately 1.6 at 0.6 $MVcm^{-1}$ for strained-Si dual-channel n-MOSFETs fabricated on a relaxed $Si_{0.50}Ge_{0.50}$ VS [12], whereas we have demonstrated comparable mobility enhancement factors at the same vertical effective field using a much lower alloy composition $Si_{0.85}Ge_{0.15}$ virtual substrate and single-channel devices. All the high mobility Δ_2 conduction band valley states are predicted to be occupied at room temperature, leading to a saturation in the mobility enhancement for virtual substrate Ge contents of approximately 20%–25% [8], [22]. Therefore, while greater gains in n-MOSFET performance are theoretically possible by increasing the Si channel strain from that caused by fabrication on a $Si_{0.85}Ge_{0.15}$ virtual substrate, further increases in the virtual substrate Ge mole fraction, as in [12], are only useful for attaining high performance strained-SiGe p-MOSFET devices. Moreover, many applications rely on the speed of the n-channel devices, and since material quality [15] and MOSFET wafer yields [23] are improved for lower Ge content virtual substrates, there are considerable benefits to using a VS alloy composition optimized for n-channel performance.

The presence of the compressively strained-$Si_{0.70}Ge_{0.30}$ layer beneath the Si channel increases the probability of Ge diffusing and reaching the strained-Si surface and interfering with the gate oxidation process compared with single-channel devices fabricated directly on a $Si_{0.85}Ge_{0.15}$ VS. Ge is rejected from a growing oxide [24], thus, nanoscale roughness develops at the strained-Si/gate oxide interface [7]. SIMS measurements confirmed a high level of Ge present at the Si–oxide interface. The impact of gate oxide interface roughness on mobility is greatest at high effective vertical fields, where surface roughness scattering dominates over phonon scattering [25]. The mean value of strained-Si–SiO_2 interface roughness of the dual-channel device was measured as 0.26 nm using high-resolution TEM, whereas, unstrained-Si devices with identical pregate oxidation cleans have gate oxide interface roughness values approximately 50% lower [26]. A high-resolution TEM image of the strained-Si–SiO_2 interface on the dual-channel structure is presented in Fig. 6. The high value of gate oxide interface roughness on the dual-channel device contributes to the reduction in mobility enhancement at higher $E_{\rm eff}$ observed in Fig. 5(b). Thus, competing mechanisms arising from the Ge mole fraction in the SiGe affect mobility. Increased Ge in the

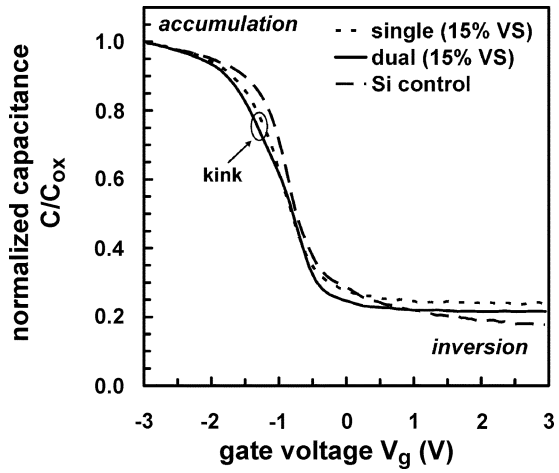

Fig. 7. *C–V* characteristics for single-and dual-channel strained-Si–SiGe MOS capacitors fabricated on $Si_{0.85}Ge_{0.15}$ virtual substrates. Bulk-Si MOS characteristics are also shown.

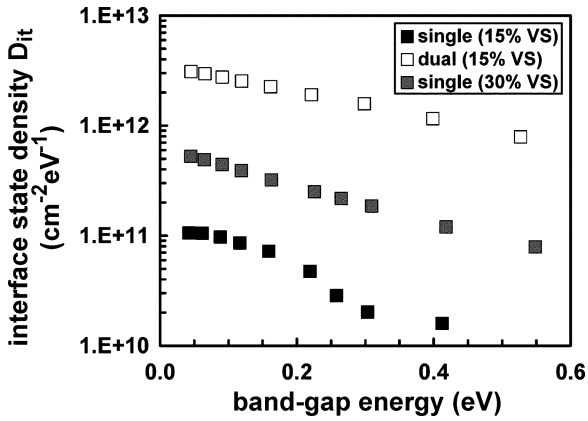

Fig. 8. Interface state density $(D_{\rm it})$ as a function of energy bandgap for single-and dual-channel MOS capacitors fabricated on a relaxed $Si_{0.85}Ge_{0.15}$ virtual substrate. Dual-channel MOS structures exhibit degraded interface trap density due to the close proximity of the high Ge-content stress-relief layer and the gate oxide. $D_{\rm it}$ for a single-channel strained-Si–$Si_{0.70}Ge_{0.30}$ structure is also shown.

virtual substrate causes greater mobility enhancements due to reduced intervalley phonon scattering, while lower Ge concentrations enhance mobility due to improved gate oxide interface roughness and reduced alloy scattering in the Si channel.

Higher values of surface roughness also correlate with increased defect levels in the gate oxide [27]. Therefore the gate oxide quality was investigated on MOS capacitors fabricated on the single-and dual-channel device wafers fabricated on $Si_{0.85}Ge_{0.15}$ virtual substrates. High-frequency capacitance–voltage (*C–V*) curves for 100 μm $\times$ 100 μm capacitors normalized against the gate oxide capacitance $(C_{\rm ox})$ are shown in Fig. 7. Good *C–V* characteristics are evident, with a kink observed in the curves when the devices are biased into accumulation. The kink arises from the confinement of holes at the strained-Si/SiGe heterointerface [28] and confirms that strain was maintained following processing. The larger valence band offset between strained-Si and strained-$Si_{0.70}Ge_{0.30}$ compared with strained-Si and relaxed $Si_{0.85}Ge_{0.15}$ causes increased hole confinement at the heterointerface of the dual-channel device compared with the single-channel device, and consequently a more prominent kink is observed for the dual-channel device on Fig. 7. Gate oxide interface trap density $(D_{\rm it})$ was measured using the conductance technique [29] on MOS capacitors fabricated on the single-and dual-channel device wafers and examined as a function of band-gap energy, as shown in Fig. 8. The data presented is representative of all measured capacitors and the dual-channel architecture demonstrates an increase in mid-gap $D_{\rm it}$ values of approximately two orders of magnitude compared with the single-channel device. Therefore, by incorporating a relatively thin compressively strained-$Si_{0.70}Ge_{0.30}$ layer for enhanced p-channel performance and robustness against strain relaxation, the gate oxide quality is severely compromised.

In addition to crosshatching, compressively strained-SiGe also exhibits periodic interface roughness undulations [30]. Both Ge out-diffusion from the compressively strained-$Si_{0.70}Ge_{0.30}$ layer into the Si channel (causing Ge pileup at the gate oxide/Si interface and nanoscale gate oxide interface roughness) and as-grown surface corrugations associated with compressed SiGe layers will contribute to the increased $D_{\rm it}$ in the dual-channel device compared with the single-channel Si–$Si_{0.85}Ge_{0.15}$ device. In order to investigate the dominating mechanism causing the higher $D_{\rm it}$ of the dual-channel devices, strained-Si single-channel devices were simultaneously fabricated directly on a thick, relaxed $Si_{0.70}Ge_{0.30}$ virtual substrate. If Ge diffusion was the primary factor behind the electrical gate oxide quality, it would be anticipated that the strained-Si–$Si_{0.70}Ge_{0.30}$ single-channel device would exhibit a higher $D_{\rm it}$ than the strained-Si–$Si_{0.70}Ge_{0.30}$/$Si_{0.85}Ge_{0.15}$ dual-channel device. In the single-channel strained-Si–$Si_{0.70}Ge_{0.30}$ device, Ge diffusion occurs primarily into the channel region during processing, whereas Ge out-diffusion from the strained-$Si_{0.70}Ge_{0.30}$ layer into the strained-Si channel is lower in the dual-channel device because Ge can additionally diffuse into the lower Ge content $Si_{0.85}Ge_{0.15}$ VS in this structure. However, Fig. 8 shows that the strained-Si–$Si_{0.70}Ge_{0.30}$ single-channel device exhibits values of gate oxide interface trap densities in between those observed on the single-and dual-channel devices fabricated on virtual substrates having 15% Ge composition. Therefore, Ge diffusion does not appear to be the dominating physical mechanism affecting $D_{\rm it}$ of the dual-channel devices, rather other properties associated with the dual-channel architecture may have a greater influence on oxide quality. AFM measurements were carried out on deprocessed devices and confirmed that the RMS surface roughness of the dual-channel device due to the strain-related undulations was 20% higher (4.5 nm; measured on 20 $\times$ 20-μm scan areas) than the single-channel device with the same $Si_{0.85}Ge_{0.15}$ VS alloy composition. We therefore propose that in our devices, surface roughness due to the compressively strained-$Si_{0.70}Ge_{0.30}$ layer makes a sizeable contribution to the increased $D_{\rm it}$ observed on the dual-channel devices. Although the surface roughness of the single-channel device fabricated on a higher Ge-content virtual substrate (30% Ge) was found to be higher than both the $Si_{0.85}Ge_{0.15}$ virtual substrates (7 nm), this is due to the cross-hatching morphology

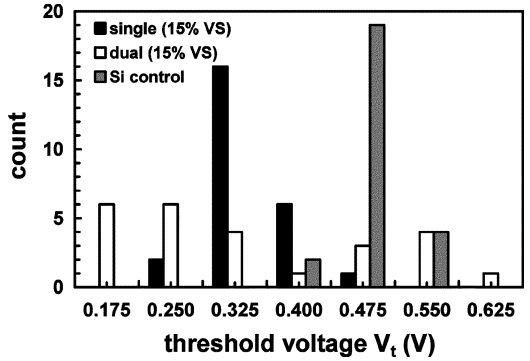

Fig. 9. Variation in threshold voltage (V_t) for single, dual and Si control 0.3-μm gate length devices. Strained-Si–SiGe devices are fabricated on a relaxed $Si_{0.85}Ge_{0.15}$ virtual substrate.

dominating values of surface roughness measured by AFM [31]. Such cross-hatching is unlikely to affect carrier transport given the large correlation length and shallow amplitudes of the roughness. Conversely, the difference in roughness observed between the single-and dual-channel architectures fabricated on 15% Ge virtual substrates is caused by the difference in the strained-channel layers and in particular the compressively strained-SiGe layer [30]. The increased surface roughness of the dual-channel device (15% VS) compared with the single-channel device (15% VS) is also commensurate with the degraded mobility enhancement of these devices at high E_{eff} [Fig. 5(b)]. Previous works have found a negligible impact of the buried strained-SiGe layer on electron mobility in 8-nm strained-Si surface channel devices [11]. The mobility degradation associated with the compressively strained-SiGe layer in our devices may be due to the relatively thin channel; although a final channel thickness of 5 nm has previously been reported to be sufficient for maximum performance gains in strained-Si n-MOS devices [8], these devices did not incorporate an underlying compressively strained-SiGe layer, thus the detrimental effects of interface scattering would be reduced.

Since oxide charge primarily affects mobility characteristics at low E_{eff} where Coulomb scattering is the mobility-limiting mechanism [21], [25], the increased D_{it} measured on the dual-channel devices may additionally explain the lower peak mobility observed for these devices compared with the single-channel strained-Si–$Si_{0.85}Ge_{0.15}$ devices at lower E_{eff} (Fig. 5). High values of D_{it} and poor gate oxide interface quality can additionally degrade the device threshold voltage (V_t) distribution [32]. A histogram showing the deviation in V_t for all 0.3 μm gate length devices across the strained-Si surface channel MOSFETs fabricated on single-and dual-channel architectures on $Si_{0.85}Ge_{0.15}$ virtual substrates and the Si control wafer is presented in Fig. 9. The single-channel devices exhibit a similar cross-wafer deviation in V_t to that demonstrated by the unstrained-control devices. However, the strained-Si dual-channel devices exhibit a much greater spread in electrical characteristics than both the single-channel and Si control n-MOSFETs. The standard deviation of V_t is three times higher for the dual-channel devices compared with the single-channel devices. These results confirm that by incorporating a SiGe compression layer into the device structure, the uniformity of some key electrical parameters and representative device performance are both compromised. However, the switching characteristics of the best performing dual-channel devices can match the n-MOSFET performance of single-channel devices (Fig. 3). Since the relationship between inversion layer mobility and effective vertical field is independent of doping at high E_{eff} [25], the increased mobility demonstrated by the single-channel device compared with the dual-channel device in Fig. 5 will not be influenced by precise channel doping in these regions.

The results presented suggest significant performance gains would need to be realized in buried p-channel devices using a dual-channel architecture compared with a strained-Si surface channel (in which hole mobility enhancements have also been reported [33]) in order to justify compromising the performance enhancements and the uniformity in key electrical parameters of n-channel devices by using such a structure with a high thermal budget process. Nevertheless, the strain-compensated dual-channel structure may enable performance enhancements in applications which use a reduced thermal budget, leading to reduced Ge diffusion. As technology nodes advance, lower thermal budgets become increasingly important for controlling dopant diffusion and minimizing short channel effects. Consequently, the detrimental impact of Ge diffusion on short-channel behavior will also decrease and the advantages of dual-channel structures are likely to increase as semiconductor manufacturing techniques develop. Alternatively, the structure may be used as a strain-compensated structure on lower Ge-composition material, thereby enabling advantages such as thicker channel layers to be realized. Reduced strain in the channel layers of such structures would enhance device performance through reduced strained-Si/strained-SiGe and strained-Si–SiO_2 interface roughness. However, the valence band offset between the two strained-layers would need to be considered if buried p-channel operation was intended since the band offset decreases with reducing Ge composition. Chemical–mechanical polishing the virtual substrates may also alleviate some of the high D_{it} values associated with the dual-channel architecture, although since surface morphology changes following high thermal budget processing [31] further work is required in this area. Nevertheless, buried channel devices allow increased design flexibility compared with surface channel devices [19]. Therefore pursuing optimized alloy composition, strain and epitaxial layer thickness for dual-channel designs remains likely to benefit many applications.

IV. Conclusion

Mobility gains exceeding 1.6 in strained-Si n-channel MOSFETs compared with bulk-Si have been demonstrated using a high thermal budget process. Improved mobility characteristics and gate oxide quality were exhibited for single-channel devices compared with devices fabricated at the same time utilizing a strain-compensated layer structure and equivalent channel strain, which can support dual-channel CMOS. Single-channel devices were found to offer significantly increased uniformity in key device parameters compared with dual-channel devices. Both device architectures had surface electron channels and

were fabricated on $Si_{0.85}Ge_{0.15}$ virtual substrates. The improved performance of the single-channel devices is considered to be due to lower interface roughness and reduced effects of Ge diffusion into the Si channel; dual-channel devices incorporated a high Ge-content strained-layer below the Si surface channel. Thus, we have shown that realizing the benefits associated with the dual-channel devices depends on a complex design parameter space and will be dependent on the electrical parameter to be optimized and device application.

ACKNOWLEDGMENT

The authors are grateful to Imperial College, London, U.K., for material growth, Southampton University, U.K., for device fabrication, and S. Bull for use of the AFM.

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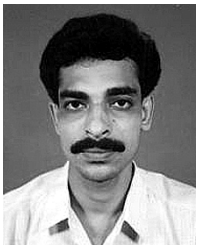

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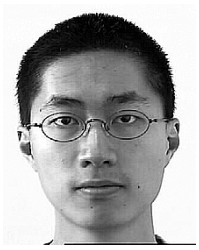

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