Modeling of the Threshold Voltage in Strained $Si/Si_{1-x}Ge_x/Si_{1-y}Ge_y(x \geq y)$ CMOS Architectures

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***Abstract*—In this paper, an analytical model of threshold voltage V_T for globally strained Si/SiGe CMOS devices using a dual-channel architecture is proposed. Since band parameters modify V_T, they are calculated and generalized for different Ge contents in a $Si_{1-x}Ge_x$ film grown on relaxed $Si_{1-y}Ge_y$ virtual substrates $(x, y < 0.7)$. A model for predicting V_T is then developed by considering device geometry and material properties, including band parameters, permittivity, and channel and substrate doping concentrations. V_T lowering due to short-channel effects is included by incorporating a voltage-doping transformation. Accuracy of the model is verified by comparing the model with the results of technology computer-aided design simulations and experiments. The model provides a physical insight for the variation of V_T for both n- and p-MOSFETs in a dual-channel architecture, and it can be generalized to be applicable to single-channel devices as well.**

***Index Terms*—CMOS, dual channel, MOSFETs, strained Si/SiGe, threshold voltage.**

I. Introduction

STRAINED $Si/Si_{1-x}Ge_x$ on a relaxed $Si_{1-y}Ge_y(x > y)$ virtual substrate (VS) dual-channel CMOS is an attractive approach to incorporate SiGe technology into conventional CMOS technology [1], [2]. In a single-channel CMOS device, the tensile strained Si (ε-Si) layer is directly grown on the $Si_{1-y}Ge_y$ VS; whereas in a dual-channel architecture, a compressively strained $Si_{1-x}Ge_x(\varepsilon\text{-SiGe})(x > y)$ and a tensile ε-Si layers are subsequently grown on a relaxed $Si_{1-y}Ge_y$ VS. The schematic cross section of the dual-channel CMOS structure is shown in Fig. 1. Such kind of layer architecture leads to a distinctive modification of the energy band structures. The compressively strained $Si_{1-x}Ge_x$ and the tensile strained Si exhibit type I and type II band alignments, respectively, with reference to the energy bands of the relaxed $Si_{1-y}Ge_y$ VS [3]. It also results in large valence band offsets (ΔE_v) at both the $\varepsilon\text{-Si}/\varepsilon\text{-}Si_{1-x}Ge_x$ and $\varepsilon\text{-}Si_{1-x}Ge_x/Si_{1-y}Ge_y$ interfaces and a large conduction band offset (ΔE_c) at the $\varepsilon\text{-Si}/\varepsilon\text{-}Si_{1-x}Ge_x$ interface, as shown in the schematic band diagrams in Fig. 2(a) and (b). This kind of band structure can be used in creating high-mobility-surface n- and buried p-channel MOSFETs on a single VS [1], [4]–[6] and is helpful in achieving greater confinement of hole in the buried channel as compared to single-channel devices, which is attributed to the large valence band offset at the $\varepsilon\text{-Si}/\varepsilon\text{-}Si_{1-x}Ge_x$, as shown in the comparison between Fig. 2(b) and (c). Furthermore, the dual-channel architecture can extend the critical thickness of the strained layer, increase thermal budget for process, and, hence, suppress strain relaxation [5], [6]. Although the advantages of dual-channel devices have been experimentally demonstrated [5], [6], one of the upcoming challenges is the precise control of V_T.

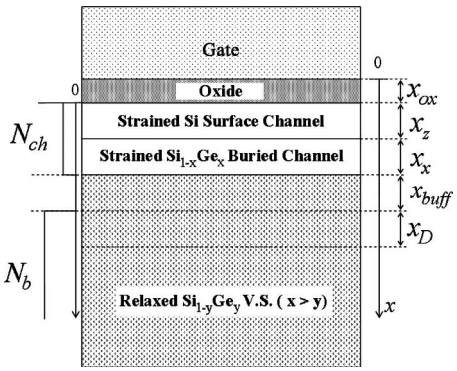

Fig. 1. Schematic cross section of a $\varepsilon\text{-Si}/\varepsilon\text{-}Si_{1-x}Ge_x$/relaxed $Si_{1-y}Ge_y(y < x)$ dual-channel CMOS architecture.

A reduction in V_T has been reported in ε-Si single-channel CMOS devices when compared with bulk-Si devices and is attributed to the change in electron affinity, presence of band offsets, and narrowed band gap of ε-Si [7], [8]. This V_T reduction is also reported in the experiment for n-MOSFET in a dual-channel architecture [5]. However, there is no analytical model available in the literature for its explanation. Moreover, there is no such model available that can address the variation of V_T for both the single- and dual-channel architectures with a Ge content in various layers in general. Consequently, it has motivated the authors to develop a new analytical generalized V_T model for n- and p-MOSFETs in $\varepsilon\text{-Si}/\varepsilon$-SiGe on a SiGe VS dual-channel architecture. The model is also applicable to predict V_T for CMOS in a single-channel architecture.

The paper is organized as follows. Section II details the method of calculation of the band parameters. In Section III, an analytical V_T model is developed for both n- and p-MOSFETs using a dual-channel architecture. The short-channel effects are incorporated using voltage-doping transformation (VDT) [9], and a condition has been reached for a specific range of source

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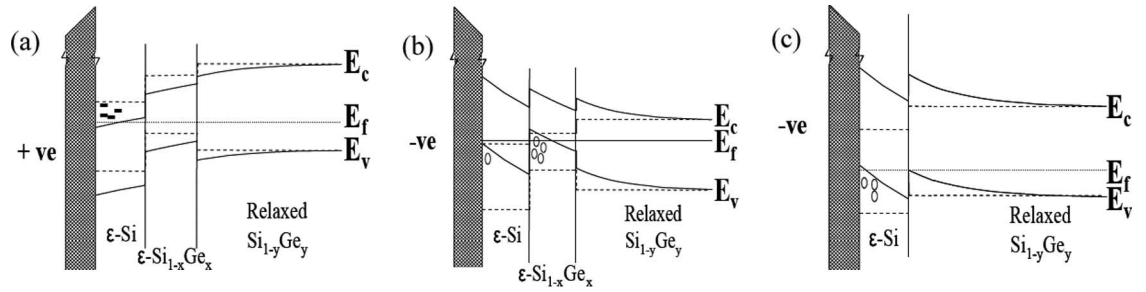

Fig. 2. Schematic band diagram for (a) n-MOSFETs and (b) p-MOSFETs in a dual-channel architecture and (c) p-MOSFETs using a single-channel architecture.

and drain voltage difference (V_D), where the model is valid. In Section IV, the validity of the model is verified by comparing results obtained from the developed model with those from technology computer-aided design (TCAD) simulations and experiments. Section V summarizes the overall findings.

II. Calculation of Band Parameters

When a thin $Si_{1-x}Ge_x$ film is epitaxially grown on a relaxed $Si_{1-y}Ge_y$ VS ($x \neq y$), the grown layer conforms to the lattice spacing of the underlying $Si_{1-y}Ge_y$ and is strained accordingly. The strain modifies the band parameters such as band gap (E_g) in the ε-$Si_{1-x}Ge_x$ film and the conduction (ΔE_c) and valence (ΔE_v) band offsets at the heterointerface. In this section, these band parameters for this SiGe heterojunction are calculated and generalized for a range of x and $y (x, y < 0.7)$ by following People's model [10]–[12]. At first, strain tensors are obtained for the strained layers from the lattice mismatch by taking into account Ge fractions in the strained layer and in the relaxed VS. These strain tensors are then substituted into the equations for calculating the components that lead to band-gap narrowing [10]. The narrowed band gap in the ε-$Si_{1-x}Ge_x$ layer can therefore be obtained by subtracting these calculated components from the relaxed $Si_{1-x}Ge_x$ band gap for the same Ge fraction. ΔE_v are obtained by following the general function in People's model based on the work of Van de Walle [12]. ΔE_c can be obtained after the E_g of the strained layers is aligned with the E_g of the relaxed VS in a band diagram. The calculated E_g, ΔE_v, and ΔE_c for various x and y values are shown in Fig. 3(a)–(c), respectively. The extracted band parameters in this paper have been verified with the available results in [11].

III. Derivation of the Model

In the structure shown in Fig. 1, x_z, x_x, and $x_{\rm ox}$ represent the thickness (in nanometers) of the ε-Si surface channel, ε-$Si_{1-x}Ge_x$ buried channel, and oxide layer, respectively. As the strained layers of the surface and buried channels are limited by their critical thickness and are normally thin, carrier depletion is assumed to be deeper than the channel regions and reaches the $Si_{1-y}Ge_y$ VS. The thickness of a buffer layer is $x_{\rm buff}$ (in nanometers). This buffer layer is assumed to be undoped, and the intrinsic doping concentrations are calculated to be 3.8×10^{10} cm^{-3} for $y = 0.1$ and 1.5×10^{11} cm^{-3} for $y = 0.3$ and can be removed from the structure by setting

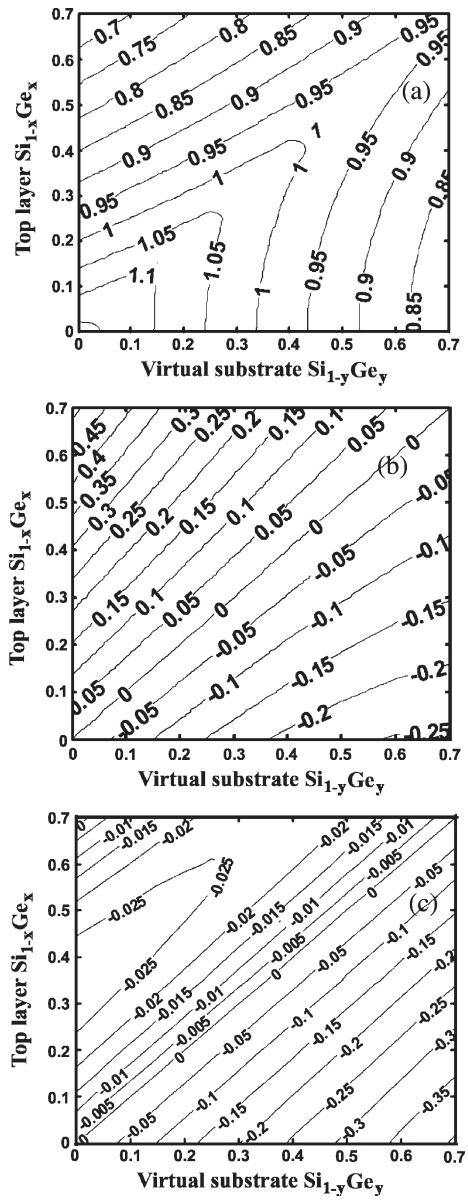

Fig. 3. Contour plots of the calculated generalized band parameters. (a) Band gap. (b) Valence band offsets. (c) Conduction band offsets.

$x_{\rm buff} = 0$ or by assuming its doping concentration to be the same as that of the VS in the model equations. The depletion depth in the substrate after the buffer layer is x_D (in nanometers). Uniform channel and substrate doping concentrations are assumed to be $N_{\rm ch}$ and N_b (in parts per cubic centimeter),

respectively. The permittivities ε in the layers are assumed to linearly vary with Ge fractions.

V_T is defined as the applied gate voltage at which strong inversion occurs in the channel. For conventional bulk-Si MOSFETs, V_T in the absence (zero) of channel (or source/drain) voltage can be expressed as

$$V_T = \phi_s + V_i + V_{\rm FB} \tag{1}$$

where ϕ_s is threshold potential in the semiconductor, V_i is depletion charge voltage, and $V_{\rm FB}$ is the flatband voltage [13].

A. V_T Modeling for n-MOSFETs in a Dual-Channel Architecture

In a dual-channel architecture, the conduction band of the ε-Si layer is always the lowest conduction band, as shown in Fig. 2(a). Therefore, the first strong inversion layer is always created in the surface channel, and hence, V_T for buried channel is irrelevant. V_T for the surface n-channel using a dual-channel architecture $(V_{\rm TN})$ is given by

$$V_{\rm TN} = \phi_{\rm SN} + V_{i,N} + V_{\rm FB} \tag{2}$$

where $\phi_{\rm SN}$ and $V_{i,N}$ are ϕ_S and V_i for *surface n-channel* devices in a dual-channel architecture, respectively.

1) Calculation of $\phi_{\rm SN}$: $\phi_{\rm SN}$ is defined as the surface potential required to create strong inversion at the oxide/ε-Si interface. As described in [14], the threshold potential for ε-Si can be approximated by taking the average between the threshold potentials of the respective channels and the relaxed $Si_{1-y}Ge_y$ VS. It should be noted that *the position of the energy bands of* ε-Si *is only decided by the amount of strain in the* ε-Si *channel layer and, hence, by the* Ge *content* (y) *only*. Thus, $\phi_{\rm SN}$ is expressed as

$$\phi_{\rm SN} = \frac{kT}{q}\left[\ln\frac{N_{\rm ch}}{n_{i,z}} + \ln\frac{N_b}{n_{i,y}}\right] - \left(\frac{|\Delta E_{c1}| + |\Delta E_{v1}|}{2}\right) \tag{3}$$

where k is Boltzmann's constant, q is the electron charge, T is the temperature in the absolute scale, and ΔE_{c1} and ΔE_{v1} denote the conduction and valence band offsets between the ε-Si channel and the relaxed $Si_{1-y}Ge_y$ VS, respectively. The notations of z and y next to the intrinsic carrier concentration n_i denote the relevant materials, i.e., ε-Si and $Si_{1-y}Ge_y$, respectively. n_i for bulk Si is expressed as

$$n_i = \sqrt{N_c N_v}\exp(-qE_g/2kT) \tag{4}$$

where N_c and N_v are the density of states for the bulk Si at conduction and valence bands, respectively. In this paper, N_c and N_v are assumed to linearly vary with the Ge fraction for the relaxed SiGe. However, these values for ε-Si are assumed to be one third of the bulk Si, whereas for ε-$Si_{1-x}Ge_x$, these values are assumed to be two thirds and one sixth of the bulk Si, respectively [15]. The E_g values for the materials are obtained from Fig. 3(a); hence, the dependence of n_i on the Ge fraction (as well as the strain) is realized.

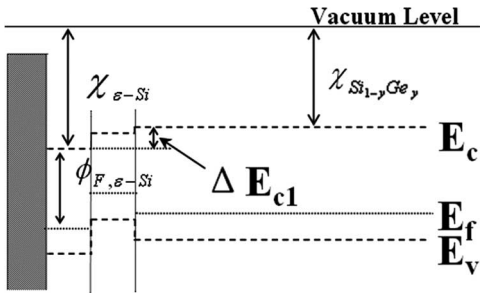

Fig. 4. Schematic band diagram showing the work function of a semiconductor in a dual-channel architecture.

2) Calculation of $V_{i,N}$: In n-MOSFETs, if a positive gate bias is applied, then it induces the negative uncompensated ionized charges in the depletion region. Such charges contribute a depletion charge voltage $V_{i,N}$, which can be solved by using a 1-D Poisson's equation [13].

At the onset of strong inversion, the potential at the SiO_2/ε-Si interface $\phi_{\rm sur}$ is equal to $\phi_{\rm SN}$ from (3). Using depletion approximation, the maximum value of x_D, i.e., the maximum depletion depth in the substrate $x_{D,\max}$, can be derived as follows:

$$x_{D,\max} = \sqrt{\frac{2\varepsilon_y}{qN_b}K + (B)^2} - B \tag{5}$$

where $K = \phi_{\rm SN} - (qN_{\rm ch}x_z^2/2\varepsilon_z + qN_{\rm ch}x_z x_x/\varepsilon_z + qN_{\rm ch}x_x^2/2\varepsilon_x)$, and $B = \varepsilon_y(x_z/\varepsilon_z + x_x/\varepsilon_x + x_{\rm buff}/\varepsilon_y)$.

$V_{i,N}$ can be calculated by estimating the total number of ionized charges in the depletion region under a MOS capacitor and is given by

$$V_{i,N} = \frac{q}{C_{\rm ox}}\left(N_{\rm ch}(x_z + x_x) + N_b x_{D,\max}\right) \tag{6}$$

where $C_{\rm ox}$ is the capacitance of the oxide layer.

3) Calculation of $V_{\rm FB}$: For bulk-Si devices, $V_{\rm FB} = \phi_{\rm ms} + Q_{\rm ox}/C_{\rm ox}$ [13], where $Q_{\rm ox}$ is a modeling parameter that combines the effects from total charges in the oxide layer (e.g., interface trap density and mobile charge), and $\phi_{\rm ms}$ is the work function difference, which is given by $\phi_{\rm ms} = \phi_m - \phi_{\rm Si}$, where ϕ_m and $\phi_{\rm Si}$ are the work functions of the gate material and semiconductor, respectively. In a dual-channel architecture, ϕ_m is unchanged, but $\phi_{\rm Si}$ must be modified for a strain-modified band structure, as shown in Fig. 4, where $\chi_{\varepsilon\text{-Si}}$ and $\chi_{Si_{1-y}Ge_y}$ denote the electron affinity of ε-Si and SiGe VS, respectively, and $\phi_{F,\varepsilon\text{-Si}}$ is the potential difference between the Fermi level (E_f) and the conduction band in the ε-Si layer (E_c). In Fig. 4, it is observed that $\phi_{\rm Si}$ is given by $\phi_{\rm Si} = \chi_{\varepsilon\text{-Si}} + \phi_{F,\varepsilon\text{-Si}}$. However, for modeling $\phi_{\rm Si}$, the average of $\chi_{Si_{1-y}Ge_y}$ and $\chi_{\varepsilon\text{-Si}}$ (instead of $\chi_{\varepsilon\text{-Si}}$) should be assumed since, after Fermi level alignment, the position of E_c of the ε-Si layer depends on ΔE_{c1} as well as the alignment of the Fermi level. Consequently, $\phi_{\rm Si}$ can be expressed as

$$\phi_{\rm Si} = \left(\chi_{Si_{1-y}Ge_y} - \frac{\Delta E_{c1}}{2}\right) + \left(\frac{E_{g,z}}{2} \pm \frac{kT}{q}\ln\frac{N_{\rm ch}}{n_{i,z}}\right) \tag{7}$$

where ΔE_{c1} should be used with a proper sign, and $E_{g,z}$ is the band gap of the ε-Si layer. The "+" and "−" signs should be chosen for n- and p-MOSFETs, respectively, from the "±" symbol in (7).

The dipole potential ($\phi_{\rm dipole}$), as described in [14], is also considered for n-MOSFET in a dual-channel architecture. It originates due to the fact that the holes will be accumulated at the ε-Si/SiGe interface under flatband conditions due to the presence of the large valence band offset and can be expressed as

$$\phi_{\rm dipole} = \frac{qN_{\rm ch}x_z^2}{2\varepsilon_z} + \frac{qN_{\rm ch}x_z L_d\sqrt{2}}{2\varepsilon_z} \tag{8}$$

where L_d is the Debye length, and $L_d = \sqrt{\varepsilon_y kT/q^2 N_b}$.

A complete expression for $V_{\rm FB}$ can now be written as

$$V_{\rm FB} = \phi_m - \left\{\left(\chi_{{\rm Si}_{1-y}{\rm Ge}_y} - \frac{\Delta E_{c1}}{2}\right) + \left(\frac{E_{g,z}}{2} + \frac{kT}{q}\ln\frac{N_{\rm ch}}{n_{i,z}}\right)\right\} - \frac{Q_{\rm ox}}{C_{\rm ox}} - \phi_{\rm dipole}. \tag{9}$$

It is noted that $\phi_{\rm dipole}$ should be excluded from (9) when V_T is calculated for bulk-Si devices. A complete expression for $V_{\rm TN}$ can be obtained by substituting (3), (6), and (9) into (2).

B. V_T Modeling for p-MOSFETs in a Dual-Channel Architecture

Due to the large valence band offset at the ε-Si/ε-$Si_{1-x}Ge_x$ interface in a dual-channel architecture, transport of holes can take place either along the buried or surface channel or along both channels, as shown in Fig. 2(b). These two channels are switched on at different gate biases, depending on the device design. Therefore, two threshold voltages in the absence of any channel bias are defined as follows:

$$\text{For the buried channel, } V_{\rm TB} = \phi_{\rm TB} + V_{i,\rm TB} + V_{\rm FB} \tag{10}$$

$$\text{For the surface channel, } V_{\rm TS} = \phi_{\rm TS} + V_{i,\rm TS} + V_{\rm FB} \tag{11}$$

where $\phi_{\rm TB}$ and $\phi_{\rm TS}$ are threshold potentials (ϕ_S), and $V_{i,\rm TB}$ and $V_{i,\rm TS}$ are depletion charge voltages (V_i) for buried and surface p-channel devices, respectively.

1) Calculation of $\phi_{\rm TB}$ and $\phi_{\rm TS}$: The definition of $\phi_{\rm TS}$ is similar to $\phi_{\rm TN}$ in Section III-A1. $\phi_{\rm TB}$ is defined as the potential required to create strong inversion in the ε-$Si_{1-x}Ge_x$ layer and can be modeled by averaging the threshold potentials of ε-$Si_{1-x}Ge_x$ channel and that of the relaxed $Si_{1-y}Ge_y$ VS. Thus, $\phi_{\rm TB}$ and $\phi_{\rm TS}$ are expressed as

$$\phi_{\rm TB} = -\frac{kT}{q}\left[\ln\frac{N_{\rm ch}}{n_{i,x}} + \ln\frac{N_b}{n_{i,y}}\right] + \left(\frac{\Delta E_{c2} + \Delta E_{v2}}{2}\right) \tag{12}$$

$$\phi_{\rm TS} = -\frac{kT}{q}\left[\ln\frac{N_{\rm ch}}{n_{i,z}} + \ln\frac{N_b}{n_{i,y}}\right] + \left(\frac{\Delta E_{c1} + \Delta E_{v1}}{2}\right) \tag{13}$$

where ΔE_{c2} and ΔE_{v2} denote the conduction and valence band offsets between the ε-$Si_{1-x}Ge_x$ buried channel and the relaxed $Si_{1-y}Ge_y$ VS, respectively.

2) Calculation of $V_{i,\rm TB}$ and $V_{i,\rm TS}$: When the potential at the ε-Si/ε-$Si_{1-x}Ge_x$ interface is more negative than $\phi_{\rm TB}$, the strong inversion is created in the buried channel, and holes reside there. These holes, as well as the depletion charges, are both considered in the model.

The potentials at specific interfaces are defined as follows: $\phi_{\rm sur}$ at the SiO_2/ε-Si interface; ϕ_H at the ε-Si/ε-$Si_{1-x}Ge_x$ interface; and $\phi(x = x_z + x_x)$ at ε-$Si_{1-x}Ge_x$/$Si_{1-y}Ge_y$ interface. $\phi(x = x_z + x_x)$ is obtained by using depletion approximation and is expressed as

$$\phi(x = x_z + x_x) = -\left(\frac{qN_b x_{\rm buff} x_D}{\varepsilon_y} + \frac{qN_b x_D^2}{2\varepsilon_y}\right). \tag{14}$$

The potential difference across the ε-Si channel, i.e., $\phi_{\rm sur} - \phi_H$, is obtained by solving Poisson's equation as follows, taking into account the ionized charges and the electric field in the ε-Si layer:

$$\phi_{\rm sur} - \phi_H = \left(\frac{x_z\varepsilon_x E_H}{\varepsilon_z} + \frac{qN_{\rm ch}x_z^2}{2\varepsilon_z}\right) \tag{15}$$

where E_H is the electric field at the ε-Si/ε-$Si_{1-x}Ge_x$ interface. E_H is expressed as

$$E_H = \frac{qN_b x_D}{\varepsilon_x}\sqrt{1 + H(\phi_H) + N_d(\phi_H)} \tag{16}$$

where $H(\phi_H)$ and $N_d(\phi_H)$ are contributions of holes and ionized donors to the electric field, respectively, and are expressed as

$$H(\phi_H) = \frac{2\varepsilon_x N_b kT}{(qN_b x_D)^2}\left[\exp\left(\frac{\phi_{\rm TB} - \phi_H}{kT/q}\right) - \exp\left(\frac{\phi(x = x_z + x_x) - \phi_H}{kT/q}\right)\right] \tag{17}$$

and

$$N_d(\phi_H) = \frac{2qN_{\rm ch}\varepsilon_x}{(qN_b x_D)^2}\left[\phi(x = x_z + x_x) - \phi_H\right]. \tag{18}$$

Derivation of E_H is detailed in the Appendix.

At the onset of strong inversion at the buried channel, $\phi_H = \phi_{\rm TB}$. By using the depletion approximation, the maximum depletion depth $x_{D,\max}$ in the substrate can be derived as

$$x_{D,\max} = \sqrt{\frac{2\varepsilon_y}{qN_{\rm ch}}(-\phi_{\rm TB}) - \frac{R_\varepsilon N_{\rm ch}x_x^2}{N_b} + (x_{\rm buff} + R_\varepsilon x_x)^2} - x_{\rm buff} - R_\varepsilon x_x \tag{19}$$

where $R_\varepsilon = \varepsilon_y/\varepsilon_x$. The maximum depletion depth ($x_{D,\max}$) is used to replace x_D in all the equations that contain x_D in the $V_{\rm TB}$ and $V_{\rm TS}$ models.

After solving Poisson's equations, $V_{i,\rm TB}$ is obtained as

$$V_{i,\rm TB} = -\left[\left(\frac{x_{\rm ox}}{2\varepsilon_{\rm ox}} + \frac{x_z}{\varepsilon_z}\right)qN_{\rm ch}x_z + \left(\frac{x_{\rm ox}}{\varepsilon_{\rm ox}} + \frac{x_z}{\varepsilon_z}\right)\varepsilon_x E_H\right]. \tag{20}$$

In (20), the first and second terms represent the voltage contributed by the ionized charges in the ε-Si layer and the charges underneath the ε-Si/ε-Si$_{1-x}$Ge$_x$ interface, respectively. To solve $V_{i,\mathrm{TB}}$ from (20), E_H is obtained by setting $\phi_H = \phi_{\mathrm{TB}}$ in (16). Similarly, a full expression of $V_{i,\mathrm{TS}}$ is expressed as

$$V_{i,\mathrm{TS}} = -\left[\left(\frac{x_{\mathrm{ox}}}{\varepsilon_{\mathrm{ox}}}\right)(qN_{\mathrm{ch}}x_z + \varepsilon_x E_H)\right]. \tag{21}$$

In (21), $V_{i,\mathrm{TS}}$ represents the voltage contributed by the charges underneath the oxide layer. At the onset of strong inversion that occurs at the SiO_2/ε-Si interface, $\phi_{\mathrm{sur}} = \phi_{\mathrm{TS}}$ and $\phi_H \neq \phi_{\mathrm{TB}}$ in (15). $V_{i,\mathrm{TS}}$ is solved as follows: 1) the expression for E_H in (16) is substituted into (15); 2) ϕ_H is now the only unknown and is solved by iterations with a first guess of $\phi_H = \phi_{\mathrm{TB}}$; and 3) E_H is obtained after substituting the calculated ϕ_H back into (16). $V_{i,\mathrm{TS}}$ in (21) can be solved with this calculated E_H.

3) Calculation of V_{FB}: Steps for calculation of V_{FB} are similar to those in Section III-A3. The differences are that the effect of the dipole potential is calculated to be insignificant in dual-channel p-MOSFETs, and the "$-$" sign is chosen from the "$\pm$" symbol in (7). Thus, V_{FB} is expressed as

$$V_{\mathrm{FB}} = \phi_m - \left(\chi_{\mathrm{Si}_{1-y}\mathrm{Ge}_y} - \frac{\Delta E_{c1}}{2}\right) + \left(\frac{E_{g,z}}{2} - \frac{kT}{q}\ln\frac{N_{\mathrm{ch}}}{n_{i,z}}\right) - \frac{Q_{\mathrm{ox}}}{C_{\mathrm{ox}}}. \tag{22}$$

The complete expression for V_{TB} is obtained by substituting (12), (20), and (22) into (10), and that for V_{TS} is obtained by substituting (13), (21), and (22) into (11). It should be pointed out that a measurable V_T in the experiment is the minimum between $|V_{\mathrm{TB}}|$ and $|V_{\mathrm{TS}}|$.

C. Calculation of the Channel-Length-Dependent V_T

To take into account the short-channel effect in the present model, the VDT is incorporated [9] since it is simple and considerably accurate. VDT suggests that the potential barrier height lowering due to the drain–source field can be modeled by assuming a reduction in the net channel doping concentration.

To incorporate VDT in the present model, the first step is to calculate the effective doping concentration N_b^* in terms of the source–drain voltage V_D, channel and substrate doping concentrations N_{ch} and N_b (considering the effect of advanced doping profile such as retrograde doping), and channel length (L_{eff}). Then, replace N_b by N_b^* into the depletion charge voltage equations; i.e., (5), (6), and (14)–(21) for the model of n- and p-MOSFETs, respectively.

Based upon the simplified VDT used in [16], N_b^* for n-MOSFETs using a dual-channel architecture by taking into account the channel and substrate doping is modified as

$$N_b^* = (N_b + N_{\mathrm{ch}}) - \frac{2\varepsilon_y V_D^*}{qL_{\mathrm{eff}}^2} \tag{23}$$

where V_D^* is the effective drain voltage, and the "$-$" sign on the right-hand side represents the product of positive V_D^* and negative q for n-MOSFETs. It is worth specifying that the net contribution from $N_b + N_{\mathrm{ch}}$ in (23) depends on the relative values of the channel and substrate doping concentrations

$$V_D^* = V_D + 2(V_{\mathrm{bi}} - \phi_{\mathrm{SN}}) + 2\sqrt{(V_{\mathrm{bi}} - \phi_{\mathrm{SN}})(V_{\mathrm{bi}} + V_D - \phi_{\mathrm{SN}})} \tag{24}$$

where V_{bi} is the built-in potential of the drain–substrate p-n junction. The second term in (23) indicates that the N_b^* decreases with decreasing L_{eff} and increasing V_D^*. As a result, V_T decreases.

To express N_b^* in p-MOSFETs, the negative and positive signs are inverted and ϕ_{SN} is replaced by ϕ_{TB} in (24). It is noted that VDT becomes invalid whenever N_b^* is assumed to have a negative value, indicating that all impurity ions are tied by the drain field and MOSFET reaches the punch-through mode. The term V_T becomes insignificant under such a condition [16]. It is important to note that VDT depends on N_b and N_{ch} as well as on V_D. Therefore, it can be used in estimating the effect of V_D on V_T for a set of given doping values. However, the variation of V_T with V_D has been reported in [9], and we have observed a similar variation. In the present model, V_D is assumed to be 0.1 V, following the values of experimental parameters. Therefore, this model is valid up to a V_D for which N_b^* is positive for given values of L_{eff}, N_b, and N_{ch}.

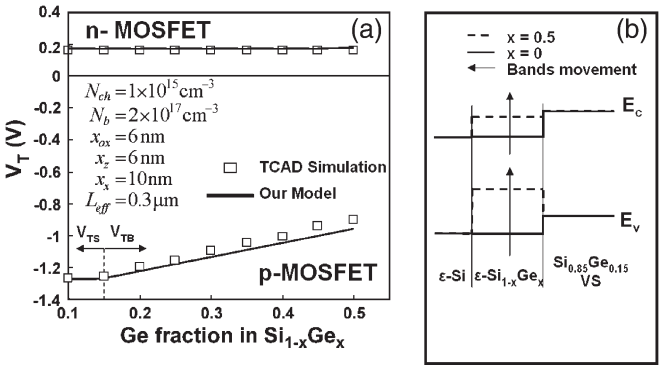

Fig. 5. (a) Comparison of V_T values extracted from the present model and TCAD simulation at different Ge fractions in a Si$_{1-x}$Ge$_x$ buried channel for the CMOS devices on a ε-Si/ε-Si$_{1-x}$Ge$_x$/relaxed Si$_{0.85}$Ge$_{0.15}$ VS architecture. (b) Schematic energy band moment for increasing Ge fraction (x) from 0 to 0.5.

IV. Results and Discussion

In Fig. 5(a), the results extracted from the present analytical model for CMOS devices in a dual-channel architecture are compared with the results obtained from TCAD simulation using Medici [17] for various Ge fractions in the ε-Si$_{1-x}$Ge$_x$ buried channel ($0.1 \leq x \leq 0.5$) on a VS that has a Ge fraction of 0.15 (Si$_{0.85}$Ge$_{0.15}$ VS). The V_T values obtained from both the analytical model and TCAD simulation for a similar set of device parameters show good agreement, indicating accuracy of the proposed model.

From the results for p-MOSFET, it is apparent that for $x > 0.15$, $|V_T|$ decreases with an increase in the Ge content (x). This is attributed to the upward movement of the valence band of the buried Si$_{1-x}$Ge$_x$ channel with increasing x as compared

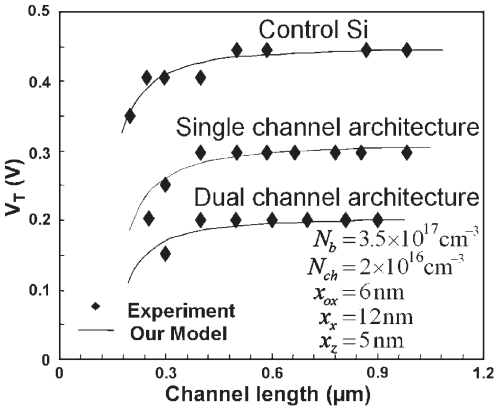

Fig. 6. Comparison of V_T values extracted from the present model with experimental data at different effective gate lengths for n-MOSFETs on control Si, ε-Si on a $Si_{0.85}Ge_{0.15}$ VS in a single-channel architecture, and ε-Si/ε-$Si_{0.7}Ge_{0.3}$ on a relaxed $Si_{0.85}Ge_{0.15}$ VS in a dual-channel architecture.

to its position at $x = 0.15$ [Fig. 5(b)]. This upward movement reduces $|\phi_{\rm TB}|$, and hence, the same number of holes can be induced for a relatively less negative gate bias in the buried channel and results in a decrease in $|V_{\rm TB}|$. This explanation is valid for $|V_{\rm TB}| < |V_{\rm TS}|$. In the regime of $x < 0.15$, the V_T value is almost constant. It is due to the fact that, in this regime ($|V_{\rm TB}| > |V_{\rm TS}|$), the positions of the energy bands of ε-Si remain unchanged by changing the Ge content (x) [Fig. 5(b)], and hence, $V_{\rm TS}$ is almost constant.

It should be noted that at $x = 0.15$, the device is in a single-channel architecture, where a type II band alignment occurred, as shown in Fig. 2(c). In the range of $0.1 \leq x < 0.15$, two type II band alignments for both tensile strained Si and $Si_{1-x}Ge_x$ layers with reference to energy bands of the VS are expected. Our V_T model should be able to extend to the devices under the condition of having a Ge content with $x < y$.

The results for n-MOSFETs in Fig. 5(a) show that $V_{\rm TN}$ is almost independent of the Ge content (x). This effect can be understood from the fact that the position of energy bands of the surface channel is independent of the Ge content (x) [Fig. 5(b)], but it depends on the Ge content (y) in the VS. Our model clearly predicts this behavior since in the equations for $V_{\rm TN}$, no parameter depends on the Ge content (x), except for ε_x. In fact, the increase in the Ge content (x) increases ε_x, which leads to a slight extension of the depletion depth, increase in ionized charges, and, hence, a slight increase in $V_{\rm TN}$ in terms of an increase in $V_{i,N}$.

In Fig. 6, the results of our analytical model are compared with the experiment for various gate lengths from 1 to 0.18 μm in n-MOSFETs using bulk-Si, single-channel, and dual-channel architectures. The details of the fabrication are given elsewhere [5]. The single-channel devices have a Ge fraction of 0.15 in the VS, whereas the dual-channel devices have a Ge fraction of $x = 0.3$ and $y = 0.15$. The thickness of ε-Si in the single-channel devices is 5 nm, whereas the thicknesses in dual-channel devices are 5 and 12 nm for the ε-Si and ε-$Si_{1-x}Ge_x$ channels, respectively. In the present model, thicknesses of 0 and 12 nm are taken for the buried channel layer (x_x) to achieve n-MOSFETs in single- and dual-channel architectures, respectively. The experimental V_T are defined at the drain current $I_D = 70$ nA/μm in I_D–V_G (gate voltage) characteristics at $V_D = 0.1$ V.

As seen in Fig. 6, the present model shows an excellent agreement to the experiment in the short-channel, as well as the long-channel, regime. Two phases of V_T shifts are observed: 1) from a control-Si to a single-channel n-MOSFET and 2) from a single-channel to a dual-channel n-MOSFET. The present model suggests two different mechanisms for the V_T shifts. The first phase of the V_T shift has been well understood, as reported in the literature [7], [8], [14], and is explained by the presence of the conduction band offset between the ε-Si and $Si_{1-y}Ge_y$ VSs, which brings the conduction band of the surface n-channel closer to the Fermi level and reduces the threshold potential $\phi_{\rm SN}$. Another source that causes this reduction is the change in oxide charges for single-channel devices [18]. To explain the second phase of the V_T shift, initially, it is referred to Fig. 5(a), where $V_{\rm TN}$ is almost independent of the Ge fraction (x). Therefore, theoretically, V_T for dual- and single-channel devices should be the same, which is not consistent with the experiment, as shown in Fig. 6. To explain this apparent inconsistency, two effects are considered: 1) the effect of setting the buried channel thickness (x_x) to 12 nm in (6) and 2) the effect of the total oxide charge.

In going from single- to dual-channel structures, a thin layer ($x_x = 12$ nm in this case) with doping lower than the substrate doping is introduced between the surface channel and VS. This additional layer increases $V_{i,N}$ by the term $N_{\rm ch}(x_z + x_x)$ in (6). In contrast, this layer provides a higher screening effect due to additional depleted charges in this layer, resulting in the reduction of $x_{D,\max}$ in (6). Since $N_b > N_{\rm ch}$, $V_{i,N}$ is reduced by this $x_{D,\max}$ reduction. Hence, V_T is reduced for dual-channel as compared to single-channel structures.

Additionally, our work in [18] has shown that the fixed oxide charges and interface state density increase with an increasing Ge fraction in the layer underneath the ε-Si layer. Therefore, the variation of $Q_{\rm ox}$ with the Ge fraction (x) is necessarily included when explaining the experimental results. The model uses the measured values (3.2×10^{11} cm^{-2} [18]) of $Q_{\rm ox}$ for calculating V_T for dual-channel devices, showing a good agreement with the experiment in Fig. 6. However, the major contribution ($\approx 70\%$) to the reduction of V_T from a single- to a dual-channel architecture comes from the reduction in the depletion charge voltage rather than from the increase in oxide charges. It is worth specifying that the experimental data are not smooth enough compared with the calculated values, which is attributed to the inherent nonuniformity in the device and wafer processing.

Fig. 7(a) compares the V_T values calculated from the present model with experimental data for various Ge fractions in the $Si_{1-y}Ge_y$ VS ($0 \leq y \leq 0.3$) for n-MOSFETs in a *single-channel* architecture. The model shows an excellent agreement even with the data for a single-channel device. The decreasing trend in Fig. 7(a) can be explained by the fact that increasing the Ge fraction (y) leads to an increase in the conduction band offset between the ε-Si and $Si_{1-y}Ge_y$ VSs, which brings the conduction band of ε-Si closer to the Fermi level and results

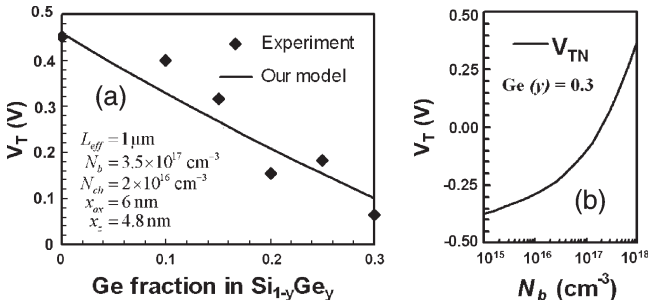

Fig. 7. (a) Comparison of V_T values extracted from the present model with experimental data for different Ge fractions in a relaxed $Si_{1-y}Ge_y$ VS (y) for n-MOSFETs in a single-channel architecture. (b) Variation of V_T with N_b for these devices with a Ge content $y = 0.3$.

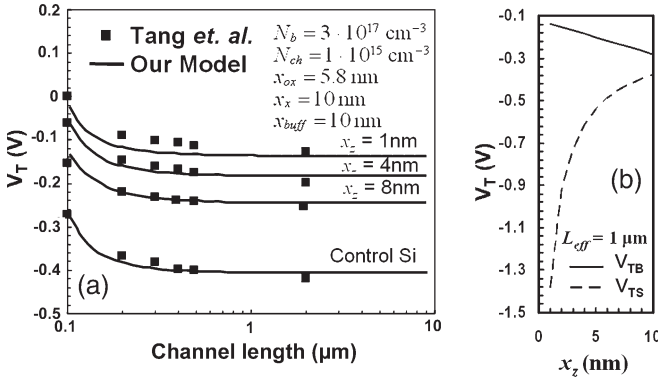

Fig. 8. (a) Comparison of V_T values calculated from the present model with experimental data [19] at different effective gate lengths $L_{\rm eff}$ for p-MOSFETs in Si/ε-$Si_{0.7}Ge_{0.3}$ on Si architectures with 1, 4, and 8 nm strained Si layer thicknesses x_z. (b) Variation of V_T with x_z for $L_{\rm eff} = 1\ \mu$m.

in the reduction of the threshold potential $\phi_{\rm SN}$, as described in (3). It also narrows the band gap in the ε-Si channel, which results in an increase in $n_{i,z}$ and, therefore, decreases the logarithmic term in (3) for $\phi_{\rm SN}$. Hence, the reduced $\phi_{\rm SN}$ allows strong inversion to occur at a lower gate bias and results in a lower V_T. Moreover, the model can estimate an increase in V_T by increasing the doping concentration N_b, as shown in Fig. 7(b).

In Fig. 8(a), the analytical model is compared with the experiment from [19] for various channel lengths ($L_{\rm eff}$) from 10 to 0.1 μm, as well as for Si cap thicknesses (x_z) from 8 to 1 nm, in p-MOSFETs using Si/ε-$Si_{0.7}Ge_{0.3}$ on the bulk-Si architecture. Good agreement between the analytical model and experimental results is obtained. The figure shows the classic V_T roll-off, which is explained by the lowering of the energy barrier with decreasing $L_{\rm eff}$ and is modeled in VDT in (23). Fig. 8(b) shows the variations of $V_{\rm TB}$ and $V_{\rm TS}$ with x_z, indicating the increase of $|V_T|$. This increase in $|V_T|$ is due to the fact that the quantum well located in the buried channel [Fig. 2(b)] is shifted away from the oxide layer by increasing x_z. For a thicker Si cap, a more negative gate bias is needed to create strong inversion in the buried channel. However, $V_{\rm TS}$ decreases with increasing x_z, which results from the significant reduction in $V_{i,\rm TS}$ (21).

The present model is used to predict the variations of V_T for different Ge fractions in the VS (y) for the n- and p-MOSFETs

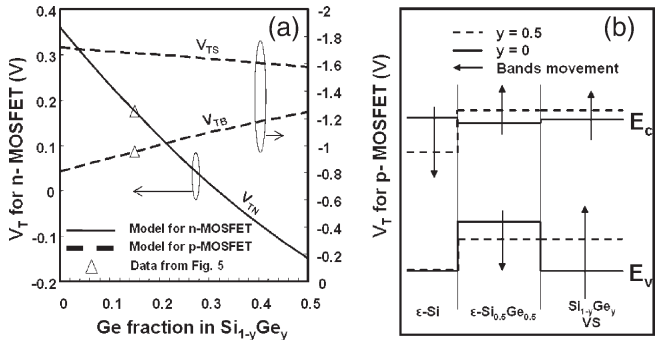

Fig. 9. (a) Plots of $V_{\rm TN}$, $V_{\rm TB}$, and $V_{\rm TS}$, calculated using the present model for different Ge fractions in the $Si_{1-y}Ge_y$ VS (y) for both n- and p-MOSFETs in a ε-Si/ε-$Si_{0.5}Ge_{0.5}$/relaxed $Si_{1-y}Ge_y$ VS dual-channel architecture. (b) Schematic energy band moment for increasing the Ge fraction (y) from 0 to 0.5.

with the $Si_{0.5}Ge_{0.5}$ buried channel in Fig. 9(a). The same device parameters as for Fig. 5 are used here. From the n-MOSFET, it is observed that $V_{\rm TN}$ decreases with increasing Ge(y), and it is consistent with the results shown in Fig. 7(a). In both cases, this $V_{\rm TN}$ lowering is attributed to the increase of the conduction band offset between the ε-Si layer and VS with the Ge fraction (y), as shown in Fig. 9(b).

From p-MOSFETs, it is observed that $|V_{\rm TB}|$ is always lower than $|V_{\rm TS}|$, and $|V_{\rm TB}|$ increases with an increase in the Ge fraction (y). This increase in $|V_{\rm TB}|$ is attributed to the fact that increasing the Ge fraction (y) (from 0 to 0.5) reduces the lattice mismatch between the $Si_{0.5}Ge_{0.5}$ buried channel layer and the $Si_{1-y}Ge_y$ VS and, hence, reduces the amount of strain in the buried channel, leading to an increase in the band gap of the buried channel and a decrease in the valence band offset between the buried channel and VS, as shown in Fig. 9(b). Consequently, a more negative gate bias is required to drive the valence band closer to the Fermi level to achieve strong inversion. Another interesting result from the figure is that $|V_{\rm TS}|$ decreases with an increase in the Ge fraction (y). It can be explained by the fact that the increase in y reduces the valence band offset between ε-Si and ε-$Si_{1-x}Ge_x$ and, hence, reduces hole confinement in the buried channel. The contribution of holes to $V_{i,\rm TS}$ is therefore reduced, as described in (21).

V. Summary

The band parameters have been generalized for different Ge contents in the $Si_{1-x}Ge_x$ layer on the $Si_{1-y}Ge_y$ VS ($x, y < 0.7$). An analytical model has been developed and verified with simulations and experimental data for n- and p-MOSFETs in both single- and dual-channel architectures. This model can predict with detailed physical explanations to the variation of V_T with design parameters, in particular, Ge fractions, layer thicknesses, channel lengths, and doping profiles. The present model will allow engineers to predict and optimize V_T for CMOS devices in both single- and dual-channel architectures in its complex design space within a range of source–drain voltage for which the effective doping concentration remains positive for a given set of values for channel length and channel- and substrate-doping concentrations.

APPENDIX
DERIVATION OF THE ELECTRIC FIELD (E_H) AT THE ε-Si/ε-$Si_{1-x}Ge_x$ INTERFACE

Poisson's equation is used to solve the electric field across the buried channel. By using depletion approximation, the charges at the onset of strong inversion in the buried p-channel are contributed by holes (p) and positive ionized donors ($N_{\rm ch}^+$). Therefore

$$\rho_{\rm charge}(x) = q\left(p + N_{\rm ch}^+\right) \tag{A.1}$$

where $\rho_{\rm charge}$ is the charge density. Since the number of holes p in the buried channel in (A.1) depends on the potential difference ϕ, the Poisson's equation to be solved becomes

$$\frac{\partial^2\phi}{\partial x^2} = \frac{q}{\varepsilon_x}\left(p + N_{\rm ch}^+\right) = -\frac{q}{\varepsilon_x}\left[N_b \exp\left(\frac{\phi q}{kT}\right) + N_{\rm ch}\right]. \tag{A.2}$$

Integrating (A.2) with the electric field and potential difference ϕ between the ε-Si/ε-$Si_{1-x}Ge_x$ and ε-$Si_{1-x}Ge_x$/$Si_{1-y}Ge_y$ interfaces, we obtain

$$\int_{\frac{\partial\phi_2}{\partial x}}^{\frac{\partial\phi_1}{\partial x}} \left(\frac{\partial\phi}{\partial x}\right) d\left(\frac{\partial\phi}{\partial x}\right) = -\frac{q}{\varepsilon_x}\int_{\phi_2}^{\phi_1}\left[N_b \exp\left(\frac{\phi q}{kT}\right) + N_{\rm ch}\right] d\phi. \tag{A.3}$$

As the electric field $\xi = -\partial\phi/\partial x$, (A.3) is derived to be

$$\xi_1^2 - \xi_2^2 = \frac{2q}{\varepsilon_x}\left\{\frac{N_b kT}{q}\left[\exp\left(\frac{\phi_1 q}{kT}\right) - \exp\left(\frac{\phi_2 q}{kT}\right)\right]\right\} + \frac{2qN_{\rm ch}}{\varepsilon_x}(\phi_1 - \phi_2). \tag{A.4}$$

The left-hand side in (A.4) is the electric field across the buried channel. Boundary conditions are assumed for the electric fields. These are $\xi_1 = \xi(x = x_z) = E_H$ and $\xi_2 = \xi(x = x_z + x_x)$, where ξ_2 can be solved using depletion approximation as follows:

$$\xi_2(x = x_z + x_x) = \frac{qN_b x_D}{\varepsilon_x}. \tag{A.5}$$

Since holes (p) are assumed to reside in the buried channel only when $|\phi_H| > |\phi_{\rm TB}|$, the boundary conditions for the potential ϕ for the right-hand side of (A.4) are

$$\phi_1 = \phi_{\rm TB} - \phi_H \quad \phi_2 = \phi_{\rm TB} - \phi(x = dx_z + x_x). \tag{A.6}$$

By substituting (A.5) and (A.6) into (A.4), (16) in Section III-B1 is finally obtained.

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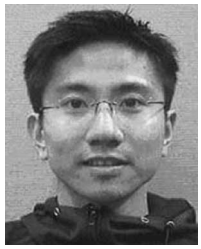

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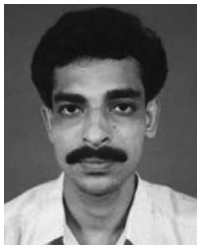

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